DS1050
RTL8711Dx Datasheet

This document provides features and information on RTL8711Dx microcontroller.

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USING THIS DOCUMENT

This document is intended for the engineer's reference and provides detailed development information.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this document.

Contents

Abbreviations

The following abbreviations apply to indicate the MCUs/platforms of Realtek.

RTL8711Dx	32-bit MCU family including RTL8711DAx/RTL8711DCx series
Real-M300 (KM4)	Arm® Cortex®-M55 instruction set compatible core based on Armv8.1-M mainline architecture, running at a frequency of up to 330MHz.
Real-M200 (KM0)	Arm® Cortex®-M23 instruction set compatible core based on Armv8-M baseline architecture, running at a frequency of up to 100MHz.
AP	Application Processor, designed for user application.
NP	Network Processor, designed for network protocol, provides network and power management services to AP.

1 Product Overview

1.1 General Description

The RTL8711Dx (including RTL8711DAx/RTL8711DCx series) is a low-power dual-band microcontroller integrating a high-performance MCU (Armv8.1-M, Cortex-M55 instruction set compatible) called Real-M300 and a low-power MCU (Armv8-M, Cortex-M23 instruction set compatible) called Real-M200. It is designed to achieve enhanced power and RF performance and low-power consumption, featuring all the characteristics of low-power chips, such as fine-grained clock gating, multiple power modes, and dynamic power scaling.

The Real-M300 (or KM4 thereafter), acting as application processor (AP), is a 3-staged pipelined 32-bit high-performance processor that bases on Armv8.1-M mainline architecture supporting Arm Cortex-M55 instruction set compatible, running at a frequency of up to 330MHz. It offers system enhancements such as enhanced debug features, floating-point computation, Digital Signal Processing (DSP) extension instructions, and a high level of support block integration for high-performance, deeply embedded applications.

The Real-M200 (or KM0 thereafter), acting as network processor (NP), is a 2-staged pipelined 32-bit low-power processor that bases on Armv8-M baseline architecture supporting Cortex-M23 instruction set compatible, running at a frequency of up to 100MHz. It is an energy-efficient and easy-to-use processor with a simple instruction set and reduced code size, and is code- and tool-compatible with the KM4 processor. It is intended for operations requiring fast response and low power consumption features, such as power management and network protocol processing.

The RTL8711Dx is a dual-band (2.4GHz and 5GHz) communication controller that integrates the specifications of Wi-Fi (Wi-Fi 4) and Bluetooth (Bluetooth 5.0). It supports 802.11 a/b/g/n wireless LAN (WLAN) network with 40MHz bandwidth. It consists of WLAN MAC, a 1T1R capable WLAN baseband, RF, and Bluetooth, providing complete Wi-Fi and Bluetooth functionalities.

A variety of peripheral interfaces, including UART, SPI, QSPI/OSPI, I2C, LEDC, etc., as well as sensor controllers (such as ADC, Cap-Touch, and Key-Scan) are integrated into RTL8711Dx devices. High-speed connectivity interfaces, SDIO and USB, are also provided. Besides, the RTL8711Dx has audio features with a dedicated digital microphone (DMIC) interface and I2S. Abundant general-purpose I/O (GPIOs) can be configured to different functions according to different IoT (Internet of Things) applications flexibly. The user-friendly development kits (SDK and HDK) are provided to customers for developing applications.

The RTL8711Dx also incorporates high-speed memories with on-chip SRAM and stacked Flash or PSRAM. A dedicated SPI Flash controller provides a flexible and efficient way to access NOR Flash (e.g., byte and block access). A multilayer AXI bus interconnect supports internal and external memory access.

The RTL8711Dx family offers devices in three different packages ranging from 48 pins to 100 pins. The included peripherals changes with the device.

1.2 Block Diagram

The functional block diagram is shown in *Figure 1-1*. This diagram provides a view of the chip's major functional components and core complexes.

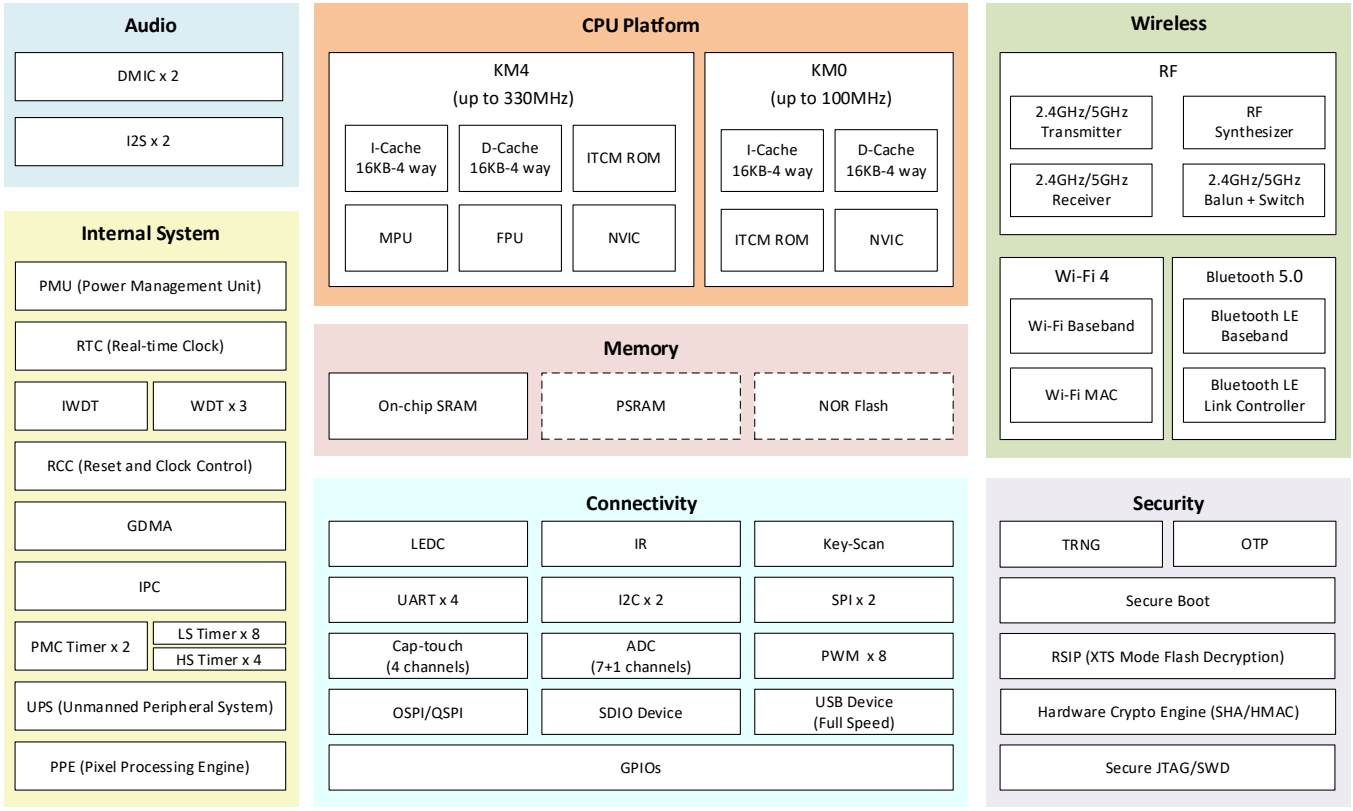


Figure 1-1 Block diagram

1.3 General Features

Table 1-1 General features

Parameter	Value
Number of Cores	2
KM4 Processor	● Arm Cortex-M55 compatible instruction set ■ I-Cache: 16K bytes ■ D-Cache: 16K bytes ● Running at a frequency of up to 330MHz ● Memory Protection Unit (MPU) with up to 8 regions with non-secure state and 4 regions with secure state ● Built-in Nested Vectored Interrupt Controller (NVIC) ● Single-precision floating point unit (FPU) ● SWD with 4 instruction breakpoints and 1 data watchpoint
KM0 Processor	● Arm Cortex-M23 compatible instruction set ■ I-Cache: 16K bytes ■ D-Cache: 16K bytes ● Running at a frequency of up to 100MHz ● Built-in Nested Vectored Interrupt Controller (NVIC) ● Physical Memory Protection (PMP) with up to 4 regions ● SWD with 2 instruction breakpoints and 1 data watchpoint
On-chip Memory	● On-chip SRAM ● PSARM (optional) ● NOR Flash (optional)
Security	● Secure boot ● Hardware crypto engine ● Whole or partial Flash decryption ● Secure JTAG/SWD ● 2K bytes OTP ● True Random Number Generator (TRNG)

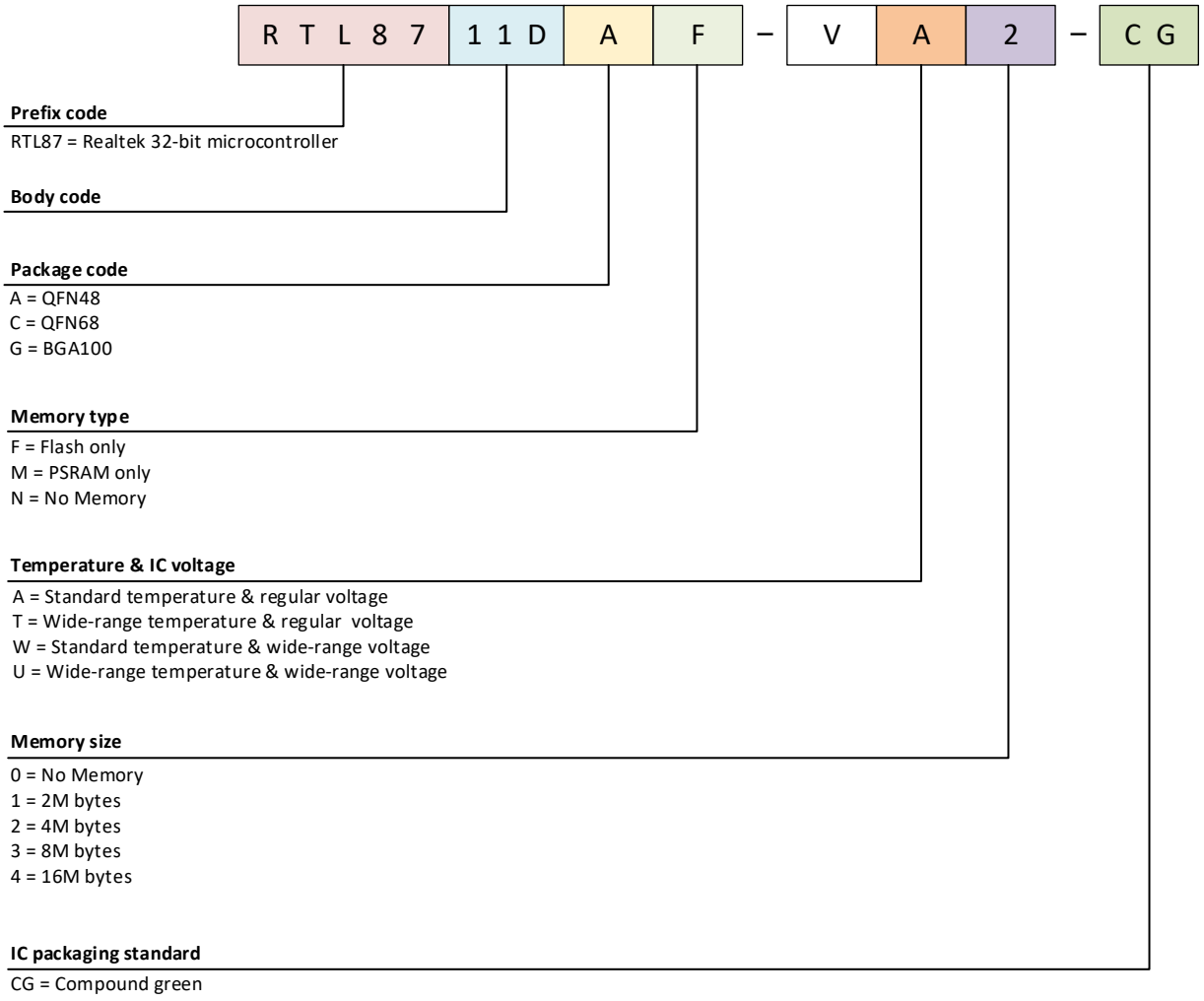
WLAN	● 802.11 a/b/g/n, 1x1, 2.4GHz & 5GHz ● 802.11n MCS0-7, 40MHz bandwidth, up to 150Mbps of data rate ● Power-saving mechanism ● Tx power (3.3V): ■ 2.4G: ◆ 11b 11Mbps: 20dBm ◆ 11g 54Mbps: 18dBm (EVM<−25dB) ◆ 11n MCS7-HT20: 17dBm (EVM<−27dB) ◆ 11n MCS7-HT40: 17dBm (EVM<−27dB) ■ 5G: ◆ 11a 54Mbps: 16dBm (EVM<−25dB) ◆ 11n MCS7-HT20: 15dBm (EVM<−27dB) ◆ 11n MCS7-HT40: 15dBm (EVM<−27dB) ● Rx sensitivity (3.3V): ■ 2.4G: ◆ 11b 11Mbps: −90.5dBm ◆ 11g 54Mbps: -78dBm ◆ 11n MCS7-HT20: −76dBm ◆ 11n MCS7-HT40: -73dBm ■ 5G: ◆ 11a 54Mbps: -77dBm ◆ 11n MCS7-HT20: −75dBm ◆ 11n MCS7-HT40: −71.5dBm
Bluetooth	● Bluetooth 5.0 specification compliant ● Compliant with Bluetooth Core Specification including LE-1M/LE-2M/LE-Coded (Long Range) ● Integrated internal Class 1, Class 2, and Class 3 PA ● Supports piconets in a scatter-net (up to 8 master roles and 3 slave roles) ● Supports LE data length extension ● Supports Link Layer privacy ● Supports LE advertising extensions ● Tx power: -10dBm ~ 10dBm, 4.5dBm typically ● Rx sensitivity: -99dBm@LE1M, -95dBm@LE2M, -102dBm@LR2, -106dBm@LR8 (not include data of spur channel 2440MHz/2480MHz)
RF	● Antenna diversity ● Internal co-existence mechanism between Wi-Fi and Bluetooth to share the same antenna
Serial Communication	● I2C x 2 ● UART x 4 ● SPI x 2
Package	● QFN48, 6mm x 6mm, 0.4mm pitch ● QFN68, 8mm x 8mm, 0.4mm pitch

1.4 Target Applications

With integrated WLAN and Bluetooth, wide range of solutions can be deployed in various fields, such as:

- Smart home
  - Lighting (dimming) control, switch and plugs
  - Home and kitchen appliances
- Industrial 4.0
- Low-power IoT
  - Smart door lock
  - Low-power Wi-Fi camera
- Smart docking and monitor
- Health-care devices
- Wearables
- Portable devices
- Gaming accessories
- Wireless audio
- Smart interactive toys

1.5 Ordering Information



Part number	Package	Flash	PSRAM	Operating Voltage	Status
RTL8711DAF-VA2	QFN48	4M bytes	-	2.97V~3.63V	
RTL8711DAM-VA2	QFN48	-	4M bytes	2.97V~3.63V	
RTL8711DCF-VA2	QFN68	4M bytes	-	2.97V~3.63V	
RTL8711DCM-VA2	QFN68	-	4M bytes	2.97V~3.63V	
RTL8711DCM-VA3	QFN68	-	8M bytes	2.97V~3.63V	

2 Chip Pinout Information

2.1 Pin Assignments

2.1.1 QFN48 Pinout

2.1.1.1 RTL8711DAF-VA

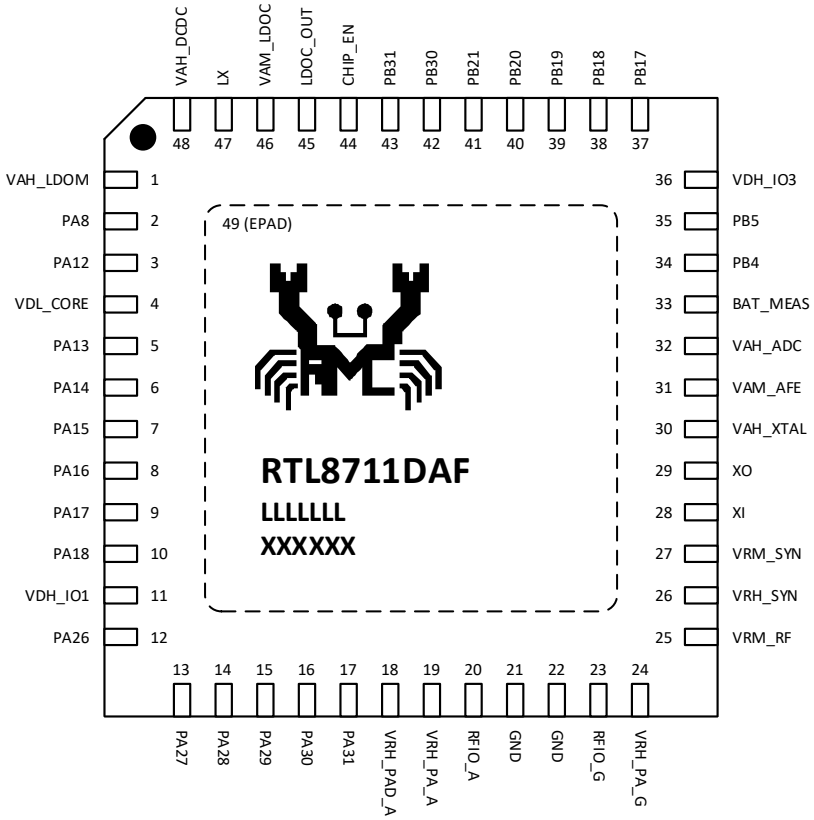


Figure 2-1 RTL8711DAF-VA series pinout

2.1.1.2 RTL8711DAM-VA

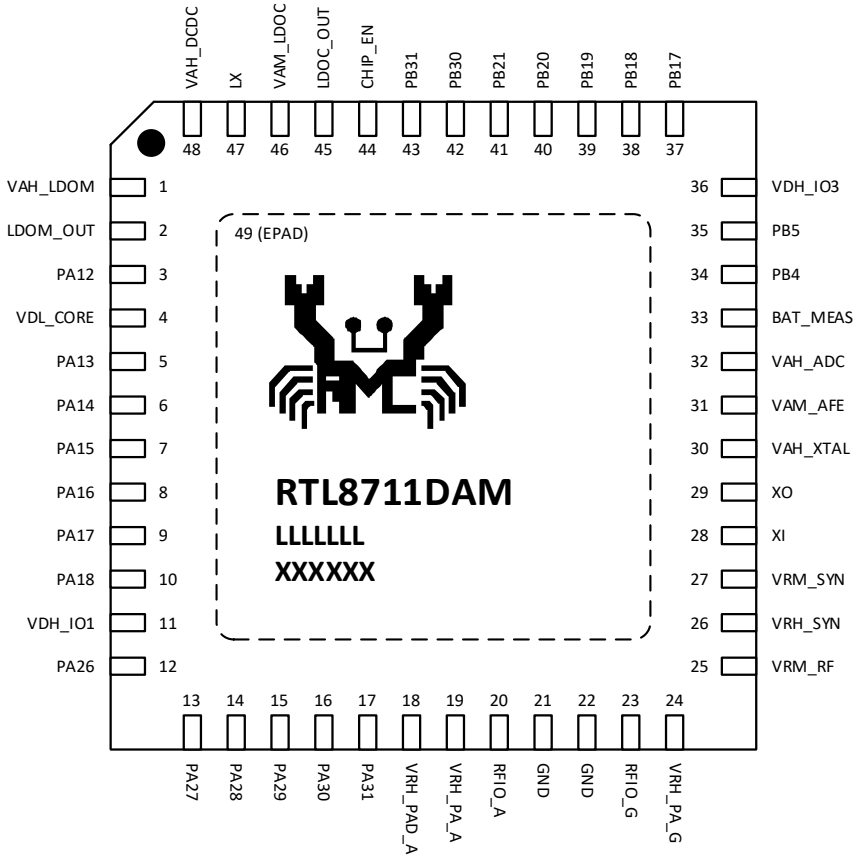


Figure 2-2 RTL8711DAM-VA series pinout

2.1.2 QFN68 Pinout

2.1.2.1 RTL8711DCF-VA

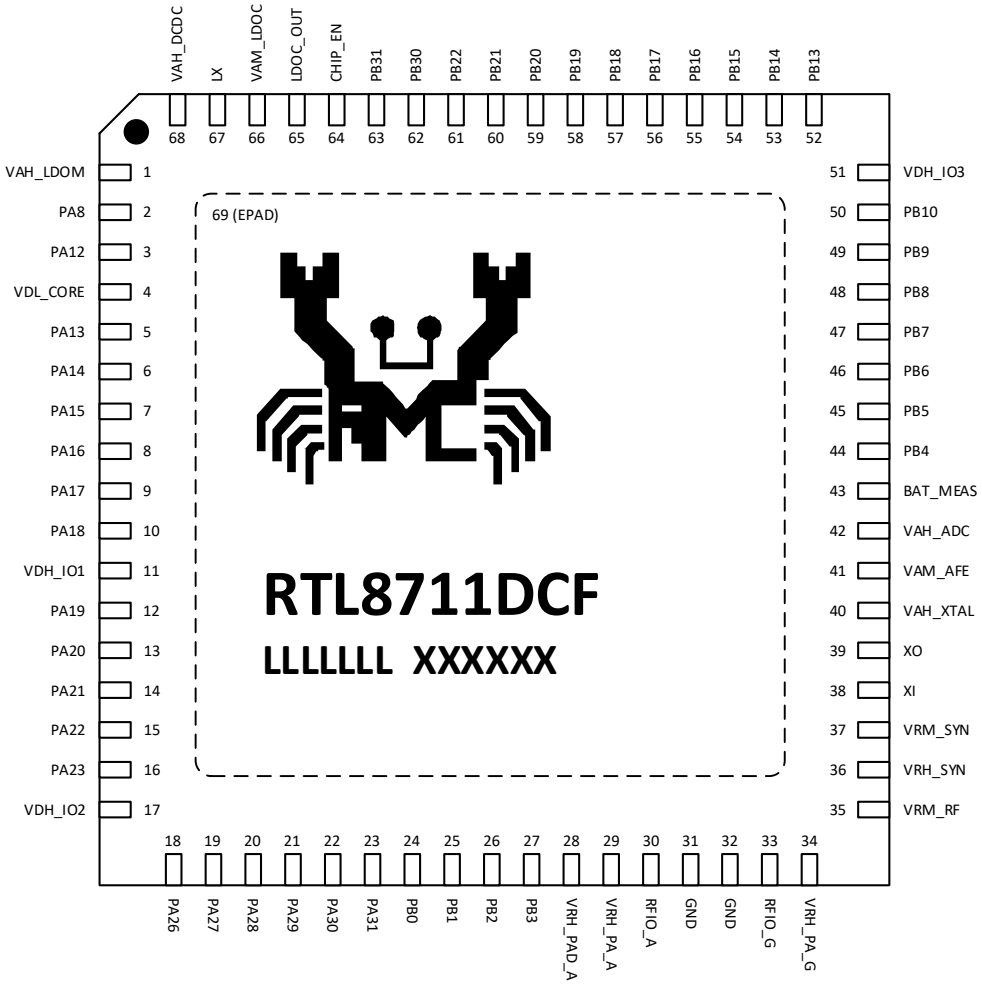


Figure 2-3 RTL8711DCF-VA series pinout

2.1.2.2 RTL8711DCM-VA

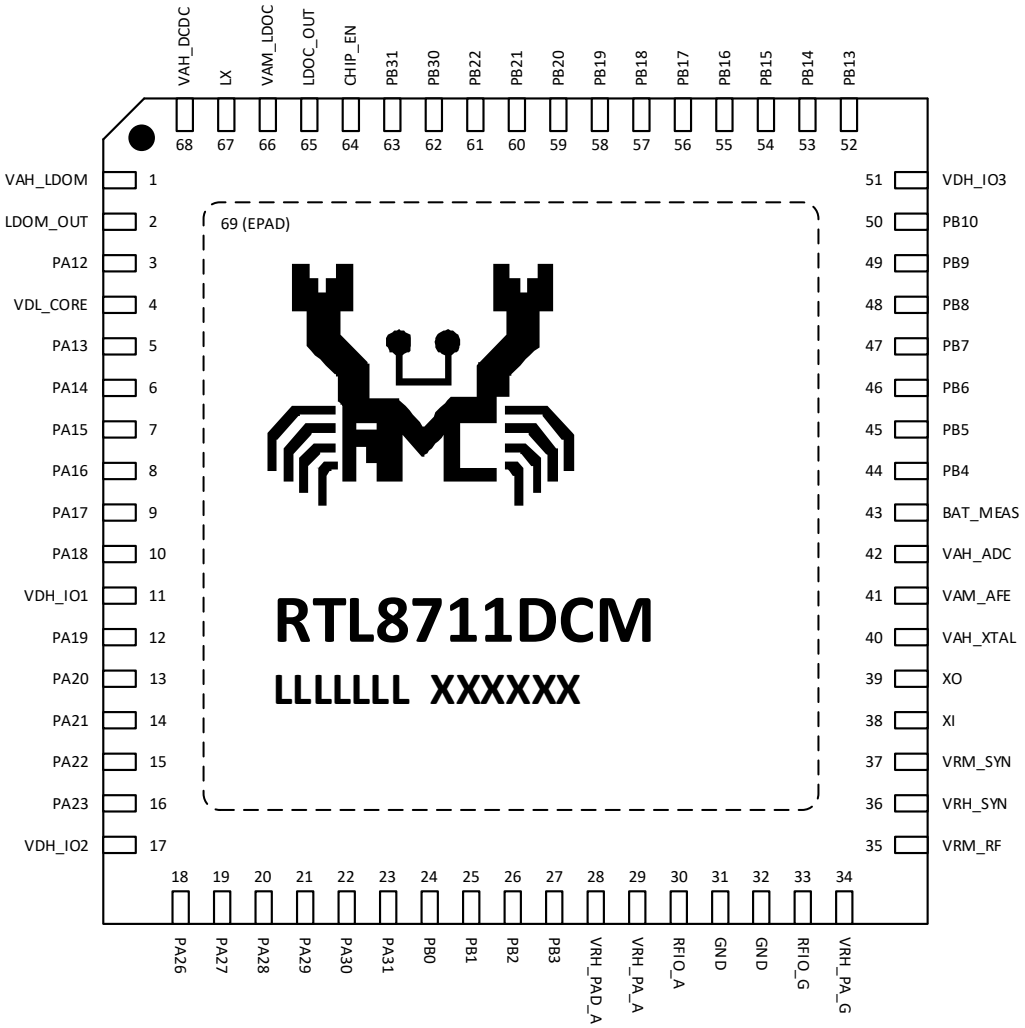


Figure 2-4 RTL8711DCM-VA series pinout

2.2 Pin Definitions

The abbreviations of pin types are listed below:

- I/O: Input/output pin
- I: Input only pin
- A: Analog signal pin
- P: Power supply pin
- G: Ground pin
- RST: Reset pin

Pin number				Pin name	Pin type	Default function[1]	Description
RTL8711DAF-VA	RTL8711DAM-VA	RTL8711DCF-VA	RTL8711DCM-VA				
1	1	1	1	VAH_LDOM	P	-	Power input for LDOM
-	-	-	2	LDOM_OUT	P	-	Power output of LDOM
2	2	2	-	PA8	I/O	GPIO	
3	3	3	3	PA12	I/O	GPIO	

4	4	4	4	VDL_CORE	P	-	Power input for the digital core domain
5	5	5	5	PA13	I/O	GPIO	
6	6	6	6	PA14	I/O	GPIO	
7	7	7	7	PA15	I/O	GPIO	
8	8	8	8	PA16	I/O	GPIO	
9	9	9	9	PA17	I/O	GPIO	
10	10	10	10	PA18	I/O	GPIO	
11	11	11	11	VDH_IO1	P	-	Power input for digital I/O power domain
-	-	12	12	PA19	I/O	GPIO	
-	-	13	13	PA20	I/O	GPIO	
-	-	14	14	PA21	I/O	GPIO	
-	-	15	15	PA22	I/O	GPIO	
-	-	16	16	PA23	I/O	GPIO	
-	-	17	17	VDH_IO2	P	-	Power input for digital I/O power domain
12	12	18	18	PA26	I/O	GPIO	
13	13	19	19	PA27	I/O	GPIO	
14	14	20	20	PA28	I/O	GPIO	
15	15	21	21	PA29	I/O	GPIO	
16	16	22	22	PA30	I/O	SWD CLK	The default function is SWD CLK, and it can be configured as PA30 after IC boot.
17	17	23	23	PA31	I/O	SWD DATA	The default function is SWD DATA, and it can be configured as PA31 after IC boot.
-	-	24	24	PB0	I/O	GPIO	
-	-	25	25	PB1	I/O	GPIO	
-	-	26	26	PB2	I/O	GPIO	
-	-	27	27	PB3	I/O	GPIO	
18	18	28	28	VRH_PAD_A	P	-	Power input for RF circuit
19	19	29	29	VRH_PA_A	P	-	Power input for RF circuit
20	20	30	30	RFIO_A	A	-	Radio transmitter output and receiver input
21	21	31	31	GND	G	-	To be connected to ground
22	22	32	32	GND	G	-	To be connected to ground
23	23	33	33	RFIO_G	A	-	Radio transmitter output and receiver input
24	24	34	34	VRH_PA_G	P	-	Power input for RF circuit
25	25	35	35	VRM_RF	P	-	Power input for RF circuit
26	26	36	36	VRH_SYN	P	-	Power input for RF circuit
27	27	37	37	VRM_SYN	P	-	Power input for RF circuit
28	28	38	38	XI	A	-	Input of 40MHz crystal clock reference
29	29	39	39	XO	A	-	Output of 40MHz crystal clock reference
30	30	40	40	VAH_XTAL	P	-	Power input for XTAL circuit
31	31	41	41	VAM_AFE	P	-	Power input for RF AFE circuit
32	32	42	42	VAH_ADC	P	-	Power input for ADC circuit
33	33	43	43	BAT_MEAS	A	-	Pin for battery voltage measurement
34	34	44	44	PB4	I/O	LOGUART Rx[2]	The default function is LOGUART Rx, and it can be configured as PB4 after IC boot.
35	35	45	45	PB5	I/O	LOGUART Tx[2]	The default function is LOGUART Rx, and it can be configured as PB5 after IC boot.
-	-	46	46	PB6	I/O	GPIO	
-	-	47	47	PB7	I/O	GPIO	
-	-	48	48	PB8	I/O	GPIO	
-	-	49	49	PB9	I/O	GPIO	
-	-	50	50	PB10	I/O	GPIO	
36	36	51	51	VDH_IO3	P	-	Power input for digital I/O power domain
-	-	52	52	PB13	I/O	GPIO	
-	-	53	53	PB14	I/O	GPIO	
-	-	54	54	PB15	I/O	GPIO	
-	-	55	55	PB16	I/O	GPIO	
37	37	56	56	PB17	I/O	GPIO	
38	38	57	57	PB18	I/O	GPIO	
39	39	58	58	PB19	I/O	GPIO	
40	40	59	59	PB20	I/O	GPIO	
41	41	60	60	PB21	I/O	GPIO	
-	-	61	61	PB22	I/O	GPIO	

42	42	62	62	PB30	I/O	GPIO	Wakeup pin. This pin should be maintained PU during reset.
43	43	63	63	PB31/TM_DIS	I/O	GPIO	Wakeup pin. The IC operating mode is determined by the level of trap pin PB31/TM_DIS during the process of power on. 1: Normal mode 0: Test mode
44	44	64	64	CHIP_EN	RST	-	Chip enable or shut-down selected pin. 1: Enable the chip 0: Shut down the chip
45	45	65	65	LDOC_OUT	P	-	Power output of LDOC & power input for the digital core domain
46	46	66	66	VAM_LDOC	P	-	Power input for LDOC
47	47	67	67	LX	P	-	DCDC output
48	48	68	68	VAH_DCDC	P	-	Power input of DCDC
49	49	69	69	GND	G	-	The exposed pad must be connected to ground plan

NOTE

[1] The pins, whose default function is GPIO, can be configured as other functions after IC boot. Refer to PM1050 (PINMUX table) for more details.

[2] If this pin is configured as a GPIO function, the LOGUART function becomes invalid.

2.3 Alternate Functions

The RTL8711Dx supports two function configuration methods: dedicated function and full-matrix function.

- For the dedicated function, the function ID is from 0 to 17. Each ID corresponds to a specific function. Only some pins configured with a function ID can be connected to the fixed signal of the corresponding function. Other pins that are not assigned this function will be invalid even if they are configured with a function ID.
- For the full-matrix function, the function ID is from 19 to 81. Each pin of PA8 ~ PA31, PB0 ~ PB31 can be configured as a function ID19~81 (only if the corresponding value of the pin under the function ID in the PINMUX table is displayed as 1). Each function ID corresponds to a certain signal of a specific function.

Compared with the dedicated function, the full-matrix function is not limited to a few specific pins when used, which increases flexibility and provides more combinations. But at the same time, the timing performance of the full-matrix function will be worse than that of the dedicated function. For specific usage restrictions, refer to the relevant content of interface timing in *Electrical Characteristics*.

Each GPIO of RTL8711Dx can be flexibly used for different functions through software configuration according to the specific usage requirements.

For the configurable functions on each GPIO, refer to *PM1050_RTL8711Dx_pin_mux.xls*.

2.4 Power Supply for Pins

Several GPIO pins belong to a specific power supply group. Each power pin may be supplied at different voltage levels as needed by the application, and can be powered by typical 1.8V or 3.3V according to different packages.

Refer to *PM1050_RTL8711Dx_pin_mux.xls* for more details on power supply pins.

3 Functional Description

3.1 Power Management

3.1.1 Power Structure

Only an external power supply is required for the RTL8711Dx. All the other required voltages can be converted and output by two embedded low-dropout regulators (LDO) and one embedded DC-DC switching regulator (DCDC).

- The DCDC outputs typical 1.25V or 1.35V for RF circuits and LDO core (LDOC) input.
- The LDOC outputs typical 0.9V or 1.0V for digital core circuits.
- The LDO memory (LDOM) outputs typical 1.8V for optional embedded PSRAM or 1.8V Flash based on different part numbers. The LDOM can also supply power for external 1.8V Flash if needed.
- When the external power supply voltage is below 1.95V, LDOM_OUT needs to be connected to an external power supply.

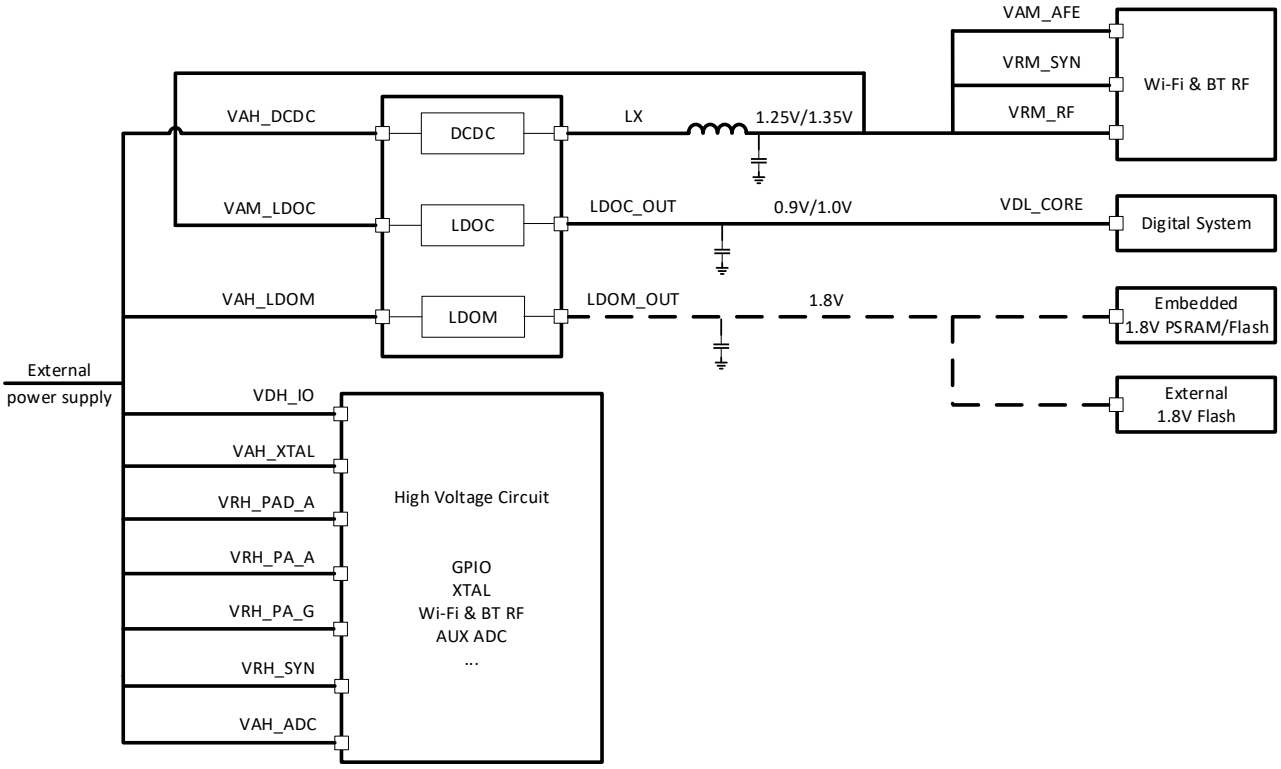


Figure 3-1 Power block diagram

3.1.2 Power Supply Supervisor

The RTL8711Dx has integrated a power-on reset (POR) circuit and a brownout detect (BOD) circuit.

3.1.2.1 Power-on Reset (POR)

The POR supervisor monitors VAH_LDOM power supply input during power on and power off.

- When VAH_LDOM is higher than V_{POR_H}, the chip releases the internal reset.
- When VAH_LDOM is lower than V_{POR_L}, the chip remains in reset mode.

Refer to *Power Sequence* for more details.

3.1.2.2 Brownout Detect (BOD)

The BOD supervisor monitors VAH_LDOM power supply input. The BOD circuit is disabled by default and can be enabled by setting the register. The BOD circuit can work in reset mode or interrupt mode and has independent falling threshold V_{BOD_L} and rising threshold V_{BOD_H}.

- When VAH_LDOM drops below V_{BOD_L}, the BOD circuit will trigger an interrupt or a reset depending on the register configuration.
- When VAH_LDOM rises above V_{BOD_H}, the BOD circuit will release the internal reset. V_{BOD_L} and V_{BOD_H} can be chosen by setting the register, but V_{BOD_H} must be set higher than V_{BOD_L}.

Refer to *Power Sequence* for more details.

3.1.3 Power Domain

The AON, SYSON, SOC are three main power domains in digital system. Functions in different power domains will be turned off differently in different power-saving modes.

By controlling the power and clock of individual functions, the RTL8711Dx can support both active mode and power saving mode. The two special power-saving modes, sleep mode and deep-sleep mode, are to achieve low power consumption with different peripherals running.

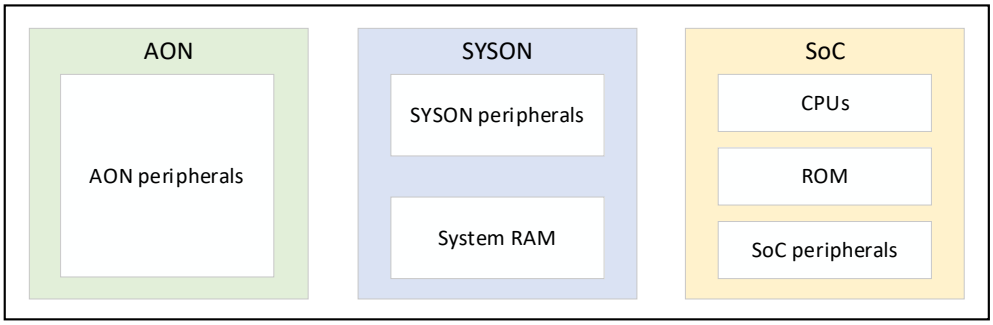


Figure 3-2 Power domain

3.1.4 Power Modes

3.1.4.1 Active Mode

In active mode, all the digital modules are powered on. Each of them can be configured as active or clock-gated, depending on the application requirement. In addition, there are individual power-down controls for some of the analog peripherals.

3.1.4.2 Sleep Mode

In sleep mode, most of the functions are power-gated or clock-gated to save power. The SoC domain will be the same with sleep mode, either power-gated or clock-gated.

Some peripherals can be used as wakeup sources, and interrupts can trigger the peripherals to wake up the system.

3.1.4.3 Deep-sleep Mode

In deep-sleep mode, all functions are powered off except the AON functions. This is to achieve ultra-lower power consumption. The system can only be woken up by the interrupt/event generated from the AON domain. When exiting from the deep-sleep mode, the system will go through normal boot flow.

Table 3-1 summarizes typical power modes supported by RTL8711Dx, which is a non-exhaustive list.

Table 3-1 Power modes

Function	**Power mode**				
	Shut down	Deep-sleep	Sleep		Active
			Power gating	Clock gating	
WLAN	OFF	OFF	Software configurable	Software configurable	Software configurable
Bluetooth	OFF	OFF	Software configurable	Software configurable	Software configurable
Processors+ Cache	OFF	OFF	OFF	Clock gating	ON
SRAM	OFF	OFF	Retention	Retention	ON

AON peripherals	RTC	OFF	Software configurable	Software configurable	Software configurable	Software configurable
	AON_WAKEPIN	OFF	Software configurable	Software configurable	Software configurable	Software configurable

Table 3-2 lists the wakeup sources of power-saving mode.

Table 3-2 Wakeup sources of power-saving mode

Power-saving mode	Wakeup source	Description
Sleep mode	WLAN	Interrupt from WLAN
	BT	Interrupt from BT
	Watchdog	Only IWDG can be a wakeup source waking from sleep mode
	IPC	The active CPU can wake up the sleeping CPU by sending IPC to the sleeping CPU
	Basic Timer	Interrupt from basic timer
	UART	Interrupt from UART
	LOGUART	Interrupt from LOGUART
	GPIO	Interrupt from GPIO
	I2C	Interrupt from I2C
	Cap-Touch	Interrupt from Cap-Touch
	ADC	Interrupt from ADC
	ADC comparator	Interrupt from ADC comparator
	SDIO	Interrupt from SDIO
	Key-Scan	Interrupt from Key-Scan
	BOR	Interrupt from BOR reset
	PWR_DOWN	Interrupt from CHIP_EN reset
	AON_TIMER	Interrupt from AON timer
	AON_WAKEPIN	Edge of AON wake pins
	RTC	Interrupt from RTC
Deep-sleep mode	AON_TIMER	Interrupt from AON timer
	AON_WAKEPIN	Edge of AON wake pins
	RTC	Interrupt from RTC
	BOR	Interrupt from BOR reset
	PWR_DOWN	Interrupt from CHIP_EN reset

3.2 Reset and Clock Control (RCC)

The RCC module manages the generation of all the clocks, as well as the clock gating and the control of the system and peripheral resets. It provides high flexibility in the choice of clock sources and allows the application of clock ratios to improve power consumption.

3.2.1 Reset Control

3.2.1.1 Reset Diagram

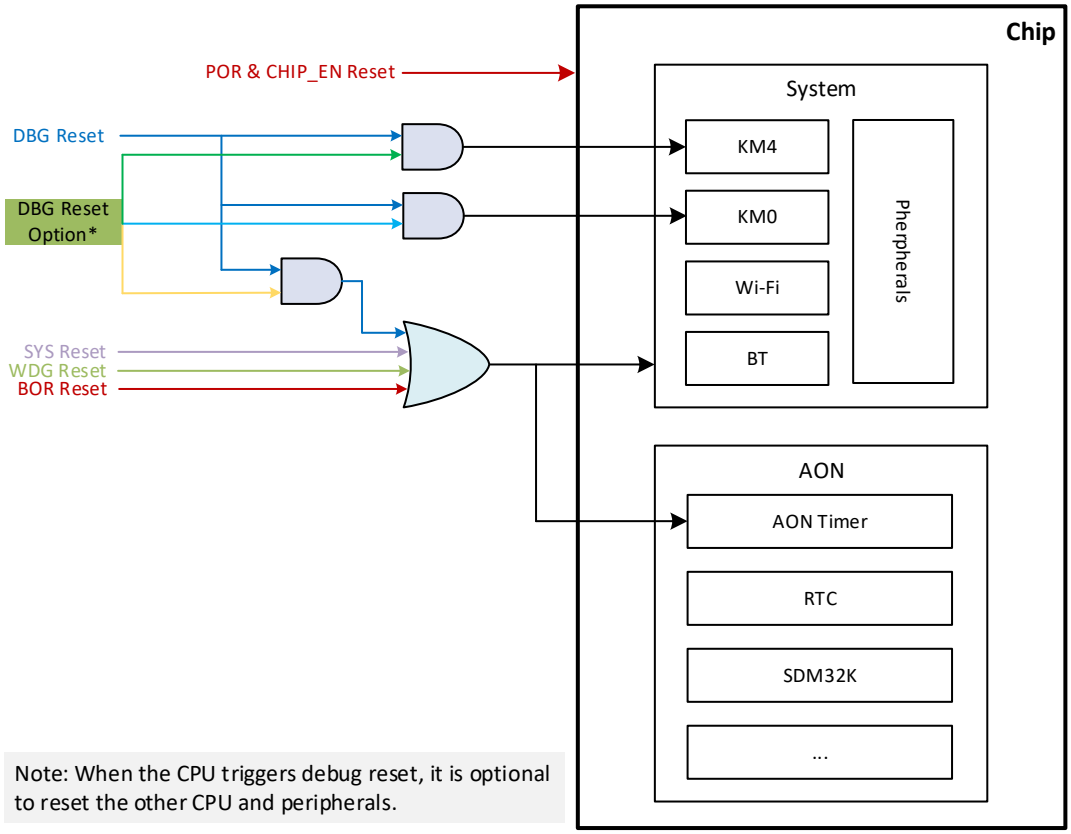


Figure 3-3 Reset diagram

3.2.1.2 Reset Type

The following reset sources or events are able to generate a reset.

Table 3-3 Reset types

Reset type	Description
POR	A power-on reset is generated when power on
BOR	A brownout reset is generated when BOR reset detected
CHIP_EN	Generated by external CHIP_EN pin
WDG	A watchdog reset is generated when watchdog timeout
SYS	A system reset is triggered by software
DBG	A debug reset is triggered by SWD debug

3.2.1.3 Reset Domain

Different reset types reset different domains:

- The power-on reset (POR) and external CHIP_EN reset can reset the whole chip.
- The BOR reset, SYS reset, and WDG reset can reset the system and AON timer.
- A debug reset is triggered by SWD debug, which will reset the CPU core definitely, and has the flexibility to reset the other CPU core and peripherals.

3.2.2 Clock Control

The clock sources of RTL8711Dx are listed below. Different clock sources can drive different functions.

- 40MHz clock based on external oscillator:
  - XTAL40M: used for peripherals directly or after frequency division.
- Internal oscillators:
  - OSC4M: provides 4MHz clock for KM0 or 2MHz clock for peripherals after frequency division.
  - OSC131K: used for input of SDM and clock for Cap-Touch and Key-Scan.
- Separate PLL:
  - PLL_SYS: 300MHz ~ 600MHz, provides the clock for KM4, KM0, and high-performance peripherals after frequency division.

3.3 CPU Architecture

There are 2 processors in RTL8711Dx for different purposes, which are KM4 and KM0.
- KM4: Application Processor (AP)
- KM0: Network Processor (NP)

The boot sequence always starts from KM4. After KM4 boots up, it will decide whether to bring up KM0 for execution.

3.3.1 KM4 Processor

The KM4 is a 3-staged pipelined 32-bit high-performance processor that bases on Armv8.1-M architecture supporting Arm Cortex-M55 instruction set compatible, and offers system enhancements such as low power consumption, enhanced debug features, floating-point computation, Digital Signal Processing (DSP) extension instructions, and a high level of support block integration for high-performance, deeply embedded applications. The KM4 achieves an optimal blend between real-time determinism, energy efficiency, software productivity, and system security that opens the door for many new applications and opportunities across diverse markets.

The KM4 processor has the following features:
- Armv8.1-M mainline architecture
- 3-stage pipeline to support the clock frequency of up to 330MHz
- Thumb/Thumb-2 technology
- 16K bytes I-Cache, 16K bytes D-Cache
- Built-in Nested Vectored Interrupt Controller (NVIC)
- Single-precision floating point unit (FPU)
- Memory Protection Unit (MPU) with up to 8 regions with non-secure state and 4 regions with secure state
- Waking up the processor from state retention power gating or when all clocks are stopped
- Non-maskable Interrupt (NMI) and physical interrupts with 8 priority levels
- Integrated wait for event (WFE) and wait for interrupt (WFI) instructions
- JTAG and Serial Wire Debug ports, up to 4 instruction breakpoints and 1 data watchpoint

The KM4 is designed to run up to 260MHz at 0.9V and 330MHz at 1.0V.

3.3.2 KM0 Processor

The KM0 is a 2-staged pipelined 32-bit low-power processor that bases on Armv8-M baseline architecture supporting Arm Cortex-M23 instruction set compatible. It is a low gate count and highly energy-efficient processor. It is an energy-efficient and easy-to-use processor with a simple instruction set and reduced code size, and is code- and tool-compatible with the KM4 processor. It is intended for applications requiring fast response and low power consumption features, such as power management and network protocol processing.

The KM0 processor has the following features:
- Armv8-M baseline architecture
- Thumb/Thumb-2 instruction subset
- 16K bytes I-Cache, 16K bytes D-Cache
- Non-maskable Interrupt (NMI) and physical interrupts with 4 priority levels
- Integrated Wait For Event (WFE) and Wait For Interrupt (WFI) instructions
- Memory Protection Unit (MPU) with up to 4 regions
- JTAG and Serial Wire Debug (SWD) ports, up to 2 instruction breakpoints and 1 data watchpoint

The KM0 is designed to run up to 100MHz at both 0.9V and 1.0V.

3.4 Memory Mapping

The RTL8711Dx incorporates several distinct memory regions. Program memory, data memory, registers, and I/O ports are organized within the same linear 4Gbytes address space. The bytes are coded in memory in Little-Endian format.

The addressable space is divided into multiple main blocks. All the memory areas that are not allocated to on-chip memories and peripherals are considered “RSVD” (reserved).

Base address	End address	Size (bytes)	Function	
0x0000_0000	0x0007_FFFF	512K	KM4 ROM (KM4 only) KM0 ROM (KM0 only)	BOOT ROM
0x0008_0000	0x000F_FFFF	512K	RSVD	
0x0010_0000	0x07FF_FFFF	127M	RSVD	Flash
0x0800_0000	0x0FFF_FFFF	128M	SPI NOR Flash	
0x1000_0000	0x1FFF_FFFF	256M	RSVD	
0x2000_0000	0x2007_FFFF	512K	SRAM	SRAM
0x2008_0000	0x200F_FFFF	512K	Shared SRAM	
0x2010_0000	0x2FFF_FFFF	255M	RSVD	
0x3000_0000	0x3FFF_FFFF	256M	RSVD	
0x4000_0000	0x40FF_FFFF	16M	High-Speed peripherals group	Peripherals
0x4100_0000	0x41FF_FFFF	16M	Low-Speed peripherals group	
0x4200_0000	0x4FFF_FFFF	224M	RSVD	
0x5000_0000	0x5FFF_FFFF	256M	RSVD	
0x6000_0000	0x6FFF_FFFF	256M	PSRAM	DRAM
0x7000_0000	0x7FFF_FFFF	256M	RSVD	
0x8000_0000	0xFFFF_FFFF	2048M	RSVD	

3.5 Memory Subsystem

The RTL8711Dx incorporates high-speed memories with on-chip SRAM and stacked Flash or PSRAM. A dedicated SPI Flash controller provides a flexible and efficient way to access NOR Flash (e.g., byte and block access). A multilayer AXI interconnect supports internal and external memory access.

The memory of RTL8711Dx consists of four types:

- ROM
- SRAM
- Flash
- PSRAM

3.5.1 ROM

The ROM address of KM4 and KM0 is the same from 0x0000_0000 to 0x0007_FFFF. However, KM4 and KM0 have physically separated internal ITCM ROMs, and each CPU can only access its own ROM.

3.5.2 On-chip SRAM

The on-chip SRAM starts from 0x2000_0000 and consists of two blocks:

- A general purposed 512KB of contiguous SRAM for system heap and application
- A dedicated 160KB of connectivity SRAM shared with Wi-Fi and Bluetooth (lower protocol stack)

All the SRAM can be accessed as bytes (8 bits), half-words (16 bits) or full words (32 bits) by KM4 and KM0, DMA engine and other AXI masters.

The entire SRAM can be disabled or enabled in the Power Management Unit (PMU) to save power, and can also enter retention mode for quickly resuming from sleep mode when the system enters sleep mode.

3.5.3 Flash

The Flash memory consists of a SPI Flash controller and a Flash memory array module. The SPI Flash controller acts as an interface between the system bus and the Flash memory device. It implements the erase and program Flash memory operations, and the read/write protection mechanisms, and accelerates code execution with a system of instruction prefetch and cache lines.

The SPI Flash controller of RTL8711Dx supports SPI NOR Flash with Single/Dual/Quad I/O pins. The I/O voltage is 3.3V or 1.8V. It can run up to 100MHz Single Data Rate (SDR) speed.

3.5.4 PSRAM

The PSRAM controller of RTL8711Dx supports high-speed hyperbus PSRAM with Double Data Rate (DDR) and 1.8V I/O voltage.

- 8-bit I/O
- Supports half sleep-mode and deep power-down mode

3.6 RF Subsystem

3.6.1 RF Block Diagram

The Radio Frequency (RF) block diagram of RTL8711Dx, including WLAN and BT modem, is given in *Figure 3-4*.

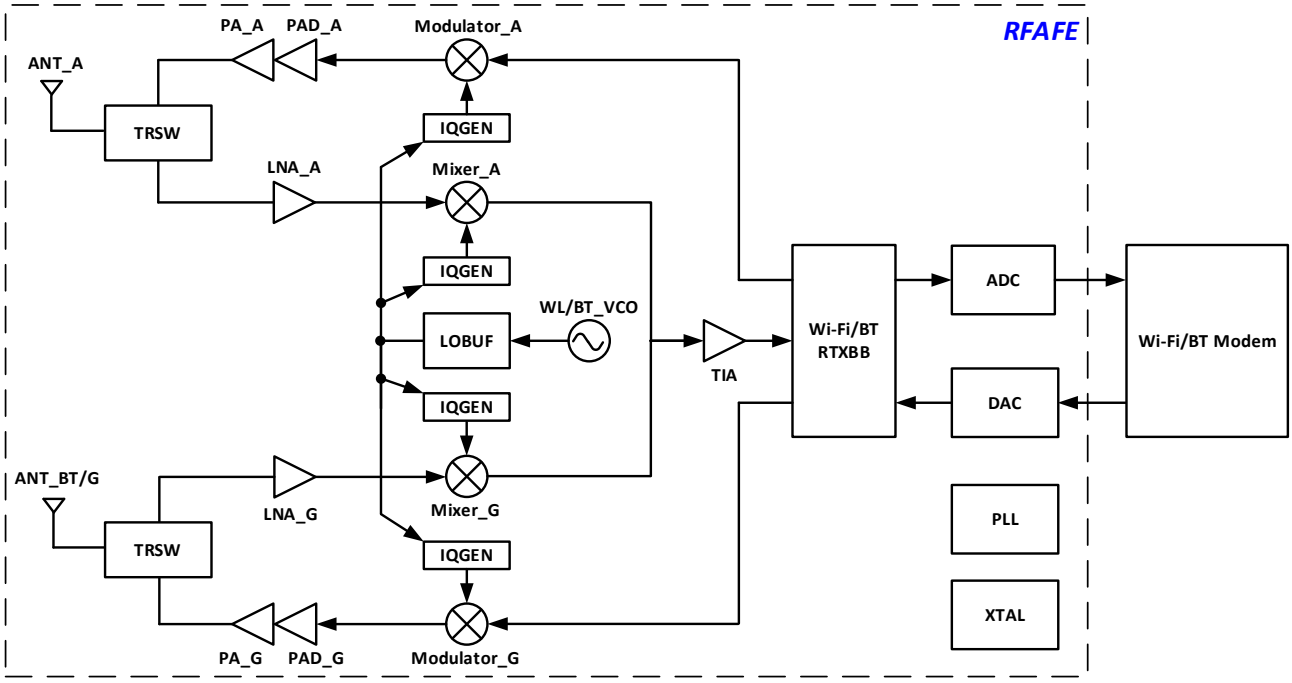


Figure 3-4 RF block diagram

3.6.2 WLAN

The RTL8711Dx includes an integrated dual-band WLAN RF transceiver that has been optimized for use in 2.4GHz and 5GHz Wireless LAN systems. It is designed to provide low-power, low-cost, and robust communications for applications operating in the globally available 2.4GHz unlicensed ISM or 5GHz U-NII bands. The transmit and receive sections include all on-chip filtering, mixing and gain control functions. The integrated on-chip baluns convert the fully differential transmit and receive paths to single-ended signal pins.

The WLAN radio subsystem of RTL8711Dx consists of the following modules:

- Receiver
- Transmitter
- Real-time calibration

3.6.2.1 WLAN Receiver

The RTL8711Dx has a wide dynamic range, direct conversion receiver that employs high order on-chip channel filtering to ensure reliable operation in the noisy 2.4 GHz ISM band or the 5GHz U-NII band. At port RFIO_G, an on-chip low-noise amplifier (LNA) in the 2.4 GHz path is shared between the Bluetooth and WLAN 2.4G receivers, while the 5GHz at port RFIO_A receiver path has a dedicated on-chip LNA. Because the NF of receiver path is lower enough, external LNA is not necessary, which can increase the receive sensitivity no more than 1dB.

3.6.2.2 WLAN Transmitter

The baseband data is modulated and up-converted to the 2.4 GHz ISM band or 5GHz U-NII band respectively. Linear on-chip power amplifiers are included, which are capable of delivering high output powers while meeting IEEE 802.11 a/b/g/n specifications without the need for external PAs. But if you do want high Tx power, external PA can be added. When using the internal PAs, closed-loop output power control is completely integrated.

3.6.2.3 Real-time Calibration

The RTL8711Dx adopts real-time and automatic on-chip calibration mechanisms to ensure that normal radio system can operate perfectly, and users do not need to do extra operations to enhance Tx/Rx performance. These calibration mechanisms that are merged into software or hardware continually compensate for temperature and process variations across components. Examples of some of these algorithms are digital correction, such as:

- I-Q compensation calibration
- Digital pre-distortion calibration for good EVM performance of the transmitter
- LO calibration for carrier leakage reduction

3.6.3 Bluetooth

3.6.3.1 Bluetooth Transceiver

The fully integrated radio transceiver is compliant with Bluetooth SIG test specifications, and designed for low power consumption, excellent transmit and receive performance in the ISM band.

- Fast AGC control to improve receiving dynamic range
- Integrated internal Class 1, Class 2, and Class 3 PA
- Supports Enhanced Power Control
- Supports Bluetooth Low Energy (BLE)

3.6.3.2 Bluetooth Transmitter

The modulator translates the baseband input signal to form the RF signal. It is designed to provide good stability and modulation characteristics.

3.6.3.3 Bluetooth Receiver

The LNA amplifies a low-energy RF signal to the desired level without significantly increasing the noise power. When input power is high, the design limits non-linearity. The Receive mixer is a device whose input is an RF signal, and the output is an IF signal. The IF signal is then passed along the IF path to the demodulator.

3.7 WLAN Subsystem

3.7.1 WLAN Baseband

The WLAN baseband of RTL8711Dx supports the following features:

- 802.11 a/b/g/n
- 802.11n MCS0-7, 40MHz bandwidth, up to 150Mbps of data rate
- Integrated 2.4GHz&5GHz PA and LNA, and T/R switch
- Integrated 2.4GHz&5GHz balun
- Adjustable transmitting power
- Supports Channel State Info (CSI)

- Supports Tx Binary Convolutional Code (BCC), and Rx BCC
- Supports Rx STBC 2x1
- Short guard interval
- Supports digital pre-distortion to enhance PA performance
- Smoothing for channel estimation
- Antenna diversity

The RTL8711Dx supports antenna diversity with an external RF switch. One or more GPIOs control the RF switch and select the best antenna to minimize the effects of channel fading.

3.7.2 WLAN MAC

The WLAN MAC of RTL8711Dx applies low-level protocol functions automatically. It supports the following features:

- Frame aggregation for increased MAC efficiency (A-MPDU)
- Low latency immediate Block Acknowledgement (BA)
- PHY-level spoofing to enhance legacy compatibility
- Power saving mechanism
- Channel management and co-existence
- Transmit Opportunity (TXOP) Short Inter-Frame Space (SIFS) bursting for higher multimedia bandwidth
- Supports Enhanced Distribution Channel Access (EDCA)
- Supports Time Synchronization Function (TSF) auto-sync
- IEEE 802.11i (WPA, WPA2, WPA3), open, shared key, and pair-wise key authentication services
- Supports AP/STA/Concurrent mode
- Support for RTS/CTS and CTS-to-self frame sequences for protecting frame exchanges

3.8 Bluetooth Subsystem

The RTL8711Dx integrates a hardware link layer controller and Bluetooth baseband, which carry out the baseband protocols and other low-level link routines, such as modulation/demodulation, packet processing, bit stream processing, frequency hopping, etc.

3.8.1 Bluetooth Baseband

The Bluetooth baseband of RTL8711Dx supports the following features:

- Compliant with Bluetooth Core Specification including LE-1M/LE-2M/LE-Coded (Long Range)
- Fast AGC control to improve receiving dynamic range
- 40MHz main clock
- Supports serial Flash for firmware storage and parameter upgrade
- Supports channel map update to dynamically detect channel quality to improve transmission quality

3.8.2 Bluetooth Link Controller

- Bluetooth 5.0 specification compliant, single mode:
  - Bluetooth Low Energy (BLE)
- Integrated MCU to execute Bluetooth protocol stack
- LE advertising extensions
- Supports piconets in a scatter-net
- Enhanced Bluetooth/WLAN Co-existence Control to improve transmission quality in different profiles
- Supports multiple Low Energy states

3.9 Security

The RTL8711Dx is designed to safely hold security-related data such as cryptographic keys and general-purpose security information with the following security techniques.

- Secure boot
- True Random Number Generator (TRNG)
- Hardware crypto engine
- Whole or partial Flash decryption
- Secure JTAG/SWD

- 2K bytes OTP

3.9.1 Secure Boot

Secure boot aims at firmware protection, which prevents attackers from modifying or replacing firmware maliciously. When the chip is powered on, the secure boot ROM executes to check the validity of the image signature.

The RTL8711Dx supports the following algorithms of secure boot:
- Signing/Authentication algorithm:
  - Ed25519
- Hash algorithm:
  - SHA512

3.9.2 Hardware Crypto Engine (IPsec)

The RTL8711Dx integrates SHA engine and AES engine, which can accelerate applications that need cryptographic functions, such as authentication, encryption and decryption. Hardware crypto engines executing these functions cannot only reduce software overhead but also save CPU and memory resources, and the processing is more secure and faster than software.

The IPsec provides basic cryptographic features:
- Authentication algorithms
  - General cryptographic hash function
    - MD5 (weak, not recommended)
    - SHA1 (weak, not recommended)
    - SHA2-224
    - SHA2-256
    - SHA2-384
    - SHA2-512
  - HMAC (Hash-based message authentication code)
    - HMAC_MD5 (weak, not recommended)
    - HMAC_SHA1 (weak, not recommended)
    - HMAC_SHA2-224
    - HMAC_SHA2-256
    - HMAC_SHA2-384
    - HMAC_SHA2-512
- Cipher (Encryption/Decryption) algorithms
  - AES-128/192/256
    - ECB (Electronic Codebook) mode (weak, not recommended)
    - CBC (Cipher Block Chaining) mode
    - OFB (Output Feedback) mode
    - CFB (Cipher Feedback) mode
    - CTR (Counter) mode (weak, not recommended)
    - GCM (Galois/Counter Mode) mode
- Four keys in OTP, two for secure mode and two for non-secure mode. The keys can be configured by software, or read from OTP by hardware engine.

3.9.3 Secure Image Protection (RSIP)

Generally, both firmware and some data are stored in Flash memory. The SPI Flash controller is used to transmit/receive data from/to SPI Flash memory. In order to protect the firmware, the code and data in Flash can be encrypted with Advanced Encryption Standard (AES) algorithm. The RSIP is mainly used for MMU and image decryption.

The RSIP consists of two parts:
- RSIP-AES: performs Flash decryption on the fly.
- RSIP-MMU: used for virtual-to-physical memory address translation.

The RSIP-AES has the following features:
- The whole or part of Flash can be decrypted.
- Encrypted Flash data is decrypted by the hardware engine on the fly.
- Optional crypto algorithm: AES-256 CTR mode or XTS mode.

- Key length is 256 bits, which should be programmed into OTP, and can be set to Read Protection and Write Protection.
- IV length is 128 bits, the higher 64 bits can be defined by users, and the lower 64 bits are decided by the address.
- Keys are auto-loaded to the hardware engine; software cannot access them after read protection is enabled.
- Keeps eight IVs in the engine, and each of the eight entries can choose a different IV and mode independently to enable decryption for specific areas.

3.9.4 True Random Number Generator (TRNG)

The TRNG integrated in RTL8711Dx is a true random number generator that provides full entropy outputs to the application as 32-bit samples.

It has the following features:
- Delivers 32-bit true random numbers, produced by a digital entropy source
- Embeds with a health test unit and an error management unit
- Two independent FIFOs, the one with low priority is for non-secure world, while the other with high priority for secure world
- Throughput of the TRNG up to about 5Mbps

3.10 Timers and Watchdogs

The RTL8711Dx includes 10 basic timers, one capture timer, one PWM timer, also two PMC timers, a RTC timer, a debug timer and several watchdog timers.

Table 3-4 Timer feature comparison

Type	Number	Counter resolution	Counter mode	Prescaler	INT generation	Sleep mode	Secure mode
Basic timer	10	32-bit	Up	×	✓	✓	✓
Capture timer	1	16-bit	Up	16-bit	✓	×	✓
PWM timer	1	16-bit	Up	16-bit	✓	×	✓

3.10.1 Basic Timer (TIM0 ~ TIM7, TIM10 ~ TIM11)

The RTL8711Dx has 10 basic timers:
- TIM0, TIM1, TIM2, TIM3, TIM4, TIM5, TIM6, TIM7: clock source is SDM32kHz
- TIM10, TIM11: clock source is XTAL1M

The basic timers also can be used as generic timers for time-based generation.

All the basic timers support:
- Resolution: 32-bit
- Counter mode: up
- Interrupt generation
- Secure mode
- Wakeup from sleep mode

3.10.2 PWM Timer (TIM8)

The RTL8711Dx has one pulse width modulation (PWM) timer (TIM8), which is a special timer to generate PWM output waveform and synchronize the multiple PWM output. Pulse lengths and waveform periods can be modulated from a few microseconds to several seconds using the timer prescaler.

The PWM timer supports:
- Channel: 8
- Clock source: XTAM40M
- Resolution: 16-bit
- Prescaler: 16-bit
- Counter mode: up
- One pulse mode with configurable default level and trigger edge
- PWM mode with polarity selection
- Interrupt generation
- Duty cycle: 0% ~ 100%
- Phase shift

- Secure mode

3.10.3 Capture Timer (TIM9)

The RTL8711Dx has one capture timer (TIM9), which can be used for a variety of purposes, including measuring the input signal pulse width or number of input signals.

The capture timer supports:
- Clock source: XTAM40M
- Resolution: 16-bit
- Prescaler: 16-bit
- Counter mode: up
- Statistic pulse width
- Statistic pulse number
- Secure mode

3.10.4 PMC Timer

Each KM4 and KM0 has one PMC timer group. One PMC timer group contains 4 timers inside, all for internal usage. They are used for different purposes in power saving flow internally, such as used for maintaining system active time or setting system sleep time.

The PMC timer has the following features:
- Clock source: SDM32kHz
- Counter mode: down
- Resolution: 32-bit
- Interrupt generation
- Wake up from sleep mode

3.10.5 Real-time Clock (RTC) Timer

The RTC module of RTL8711Dx is powered by VDH_RTC individually, which can ensure that the time data recorded by RTC will not be lost when all other power supply pins are powered off. The RTC timer keeps counting where only VDH_RTC is powered.

When all other power supply pins except VDH_RTC are powered off, the RTC timer has the following features:
- Record the RTC timing data before power off.
- Continue to keep timing.
- No calibration mechanism for RTC counting.

The VDH_RTC power pin only pins out on the BGA100 package and can be powered independently from other power supplies in the system. On other packages, the VDH_RTC power pin is bound to other power supplies of the system and cannot be powered independently.

3.10.6 Debug Timer

Debug timer is a common timestamp for all debug messages originating from all on-die processors and processor execution domains (application, kernel and firmware). It also includes a lock-free increment counter. It features:
- A simple 32-bit wrap timer
- A lock-free counter

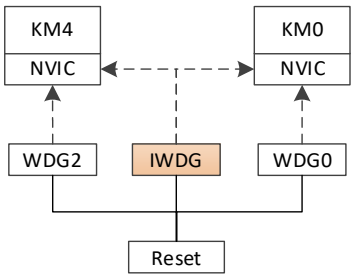
The counter is enabled by default. The counter wraps around to zero and continues to count once it reaches 32'hFFFFFFFF. A write to the timestamp will set the current value of it, however, it must continue to increment at the base of the new setting value if the writing happens when the counter is active.

The debug timer has two types of clock sources: XTAL and internal 32K. The XTAL clock may be gated in sleep mode. If users select XTAL as the clock source in sleep mode, the debug timer will stop counting, and all the registers will be maintained. The counter will resume the increment immediately after XTAL resumes. Users can select 32K as the clock source in sleep mode; however, the counter itself needs 220us to switch the clock before continuing counting. In this period, writing to this IP is not allowed. All the registers will be reset to the initial values after wakeup from deep-sleep mode.

3.10.7 Watchdog Timer

The RTL8711Dx includes three watchdog timers: one independent watchdog timer (IWDG) and two system watchdog timers (WDG).

- IWDG: an independent watchdog timer for KM0 and KM4
- WDG0: a watchdog timer for KM0
- WDG2: a watchdog timer for KM4



All the watchdog timers can trigger the reset of the corresponding CPU or the whole system.

Once enabled, the watchdog timers cannot be disabled.

3.10.7.1 Independent Watchdog Timer (IWDG)

The independent watchdog timer (IWDG) is powered by always-on power and always-on clock source, meaning that it can stay active even when the core power or crystal fails. Also, IWDG can be configured to start by hardware at the very beginning of the reset. It features:

- Powered by always-on power and always-on clock source
- Once enabled, cannot be disabled
- Can wake up the system from sleep mode with an early interrupt
- Can reset the whole system even in sleep mode
- An optional early interrupt can be generated at a programmable time prior to watchdog timeout
- Gates automatically when the KM0 or KM4 is in debug mode
- Can be configured to run or gate in sleep mode
- A separate wake reason for each watchdog timer

3.10.7.2 System Watchdog Timer (WDG0, WDG2)

The power and clock of the system watchdog timer are protected by itself. Once the watchdog timer is enabled, the processor cannot shut off the watchdog timer's power and clock again. It features:

- An optional early interrupt can be generated at a programmable time prior to watchdog timeout
- Watchdog gates automatically when the processor is in debug mode
- Gates and maintains settings in sleep mode
- Window protection function and timeout cannot be changed anymore once WDG is enabled.
- A separate boot reason for each watchdog timer

3.11 Unmanned Peripheral System (UPS)

The Unmanned Peripheral System (UPS) can be regarded as a network that lets the different peripheral modules communicate directly with each other without the participation of MCU. With UPS, the participation of software can be minimized to avoid the time error caused by software operation while realizing the control of light dimming. The two sides communicating through UPS are called producer and consumer, among which the producer is the peripheral module sending out signal, and the consumer is another peripheral module that applies corresponding actions according to the received signal. It features:

- Producer and Consumer
- Configurable signal source
- Configurable input reverse
- Positive edge detection
- Various dimming signal types

3.12 Direct Memory Access Controller (DMAC)

The RTL8711Dx has a DMAC, which allows peripheral-to-memory, peripheral-to-peripheral, memory-to-peripheral, and memory-to-memory

transactions without the participation of CPU. Each DMA stream provides unidirectional DMA transfers for a single source and destination. It features:

- Up to eight independent channels, with programmable priority
- FIFO per channel for source and destination
- Programmable flow control at block transfer level (source, destination or DMAC)
- Programmable source and destination for each channel
- Transaction: supports single and burst transaction mode
- DMA transfer: supports single-block and multi-block transfer
- Secure mode supports secure transfer mode
- Power save: support DMAC low power mode (internal clock gating)
- Supports for disabling channels without data loss
- Supports for suspension of DMA operation

3.13 Audio

The audio module is divided into two parts: DMIC interface and I2S. The functions and features are described below.

3.13.1 Digital Microphone (DMIC) Interface

The audio module integrates two DMIC interfaces.

- 8kHz/11.025kHz/12kHz/16kHz/22.5kHz/24kHz/32kHz/44.1kHz/48kHz/88.2kHz/96kHz for DMIC interface
- Configurable 0-5 band EQ
- Adjustable digital volume control
- For digital volume control, supports zero-crossing detection to minimize audible artifacts
- DC remove function

3.13.2 Inter-IC Sound (I2S0, I2S1)

The audio module integrates two I2S interfaces.

- Supports I2S normal, left-justified mode, etc.
- Supports up to 8-channel I2S transmitter by TDM or PCM mode
- Audio data word length: 16/20/24/32 bits
- Channel length: 16/20/24/32 bits
- Works in master and slave mode
- In 2 channels mode, fs supports up to 384kHz

3.14 Inter-Processor Communication (IPC)

The inter-processor communication (IPC) hardware is designed to make any two CPUs communicate with each other. The IPC provides a set of registers for each processor that facilitates inter-processor communication via interrupts. Interrupts may be independently masked by each processor to allow polled-mode operation.

The IPC communication data must be located in common memory. It features:

- Status signaling for the 32 channels (16 channels for Tx and 16 channels for Rx)
  - Channel empty/full flag, also used as a lock
- Four sets interrupt lines per processor
  - Two sets for Rx channel full (communication data posted by sending processors)
  - Two sets for Tx channel empty (communication data retrieved by receiving processors)
- Interrupt masking per channel
  - Channel Tx empty mask
  - Channel Rx full mask
- 64 hardware semaphores for the atomic operation of shared resources

3.15 Universal Serial Bus (USB) Interface

The USB module operates as a full-speed only USB 2.0 device. It allows data exchange with a USB host and allows customization of device descriptors via software configuration.

It features:
- USB 2.0 full-speed device mode
- Software-configurable internal DMA mode or slave mode
- Up to 6 endpoints, including:
  - Two bidirectional control endpoints for endpoint 0 and endpoint 5
  - Two IN endpoints for endpoint 1 and endpoint 3, with one and only one periodic IN endpoint for isochronous IN transfer
  - Two OUT endpoints for endpoint 2 and endpoint 4
- Up to 768 data FIFO depth with 35-bit per FIFO entry, supports dynamic FIFO sizing:
  - Up to 480 Rx FIFO depth, shared with all OUT endpoints
  - Up to 256 periodic Tx FIFO depth, dedicated to the periodic IN endpoint, i.e. the ISOC IN endpoint
  - Up to 32 non-periodic Tx FIFO depth, shared with all non-periodic IN endpoints

3.16 Secure Digital Input and Output (SDIO)

The SDIO device supports the following features:
- Full compliance with SDIO card specification version 2.0:
  - 1-bit and 4-bit mode
  - Default speed mode (25MHz) and high-speed mode (50MHz)
- Partial CCCR registers are configurable
- SDIO INIC mode (SDIO to Wi-Fi transformation)
- Internal DMA supported
- Interrupt control
- 3.3V/1.8V operating voltage

3.17 General-Purpose Input/Output (GPIO)

The GPIO supports the following features:
- Separate data register and data direction register for each signal
- Read back the data on external pads using memory-mapped registers.
- Independently controllable signal by bits
- Interrupt mode for each pin
  - Level sensitive: active-high level or active-low level interrupt
  - Edge trigger: rising edge, falling edge or both edges
- Option to generate single or multiple interrupts
- Configurable de-bounce time up to 8ms to de-bounce interrupts
- Level interrupt synchronization

Each of the GPIO pins can be dynamically configured by software as output or input. GPIO pins that are not connected to a specific peripheral function are controlled by the GPIO registers. Most of the GPIO pins are shared with digital or analog alternate functions.

3.18 Pixel Processing Engine (PPE)

The PPE supports alpha blending and scale function. It processes pixel data and transfers data from the input layer to the result layer. It has 3 input layers and 1 result layer.

It supports the following features:
- Alpha blending:
  - Up to 3 layers alpha blending
  - Variable pixel start position
  - Variable window size
  - Variable line length
  - Color keying
  - Multi-frame auto-reload
  - Multi-frame link list
- Scale function
  - Up to 16 times scale up/down using a bilinear interpolation algorithm
  - Variable window size
  - Variable line length
  - Color keying

  - Multi-frame auto-reload
  - Multi-frame link list
- Interrupt control
- Abort, suspend and resume pixel processing
- Supports up to 54-pixel formats such as ARGB8888, RGB5665
- Variable access
  - Input layer pixel data sources can be PSRAM, SRAM, Flash
  - Result layer pixel data destination can be PSRAM, SRAM, QSPI

3.19 Inter-integrated Circuit Interface (I2C0, I2C1)

The RTL8711Dx embeds two I2C interfaces (I2C0, I2C1), which handle communications between the RTL8711Dx and the serial I2C bus. It controls all I2C bus-specific sequencing, protocol, arbitration and timing. The design of RTL8711Dx I2C aims at sensor-hub applications in low-power or battery-powered productions. Essential features of the I2C bus protocol should be provided for acquiring or controlling external sensor data.

The I2C interface supports:
- Two-wire I2C serial interface – a serial data line (SDA) and a serial clock (SCL)
- Three-speed modes
  - Standard Speed, up to 100Kbps
  - Fast Speed, up to 400Kbps
  - High Speed, up to 3.4Mbps
- Master or Slave I2C operation
- Transmitter or Receiver
- Transmit and receive FIFOs with a depth of 16 and a width of 12-bit
- Multi-master ability including bus arbitration scheme
- Clock stretch in master/slave mode
- 7-bit or 10-bit addressing mode, 7-bit or 10-bit combined format transfer
- Manual START/RESTART/STOP bit control
- Supports General Call, NULL DATA, START BYTE transfer protocol
- Component parameters for configurable software driver support (programmable SDA hold time, slave address, SCL duty cycle, etc.)
- Filter to eliminate the glitches on signals of SDA and SCL, programmable digital noise filter
- Status flags (Bus busy flag, activity flag, FIFO status flag, etc.) and Error flags (arbitration lost, acknowledge failure, etc.)
- Slave Mode Dual Own Address
  - Slave 1 supports 7-bit or 10-bit address mode
  - Slave 2 only supports 7-bit address mode
- Operation mode
  - Polling mode
  - Interrupt mode

3.20 Universal Asynchronous Receiver/Transmitter (UART0, UART1, UART2, LOGUART)

The UART offers a flexible means of full-duplex data exchange with external equipment, requiring an industry-standard NRZ asynchronous serial data format. It provides a very wide range of baud rates using a fractional baud rate generator. Low power Rx mode is implemented by monitoring Rx baud rate error and own frequency drift.

3.20.1 UART0 ~ UART2

Except the LOGUART, the RTL8711Dx has embedded three general UART interfaces:
- UART0: 4-wire
- UART1: 2-wire
- UART2: 4-wire, reserved to control BT HCI UART. If BT function is not enabled, UART2 can be used as normal UART.

These UARTs have the following features:
- Various UART formats: 1 start bit, 7/8 data bits, 0/1 parity bit and 1/2 stop bits
- Fractional baud rate
  - Up to 8Mbps within high-speed mode (XTAL 40MHz)
  - Up to 4Mbps within low-power mode (XTAL 20MHz)

  - Up to 115.2kbps within low-power mode (OSC 2MHz)
- Separated clocks for Tx path and Rx path
  - Tx path: XTAL 40MHz
  - Rx path: XTAL 40MHz, XTAL 20MHz, OSC 2MHz
- 11-bit * 16 asynchronous Transmit/Receive FIFO
- Configurable auto-flow control
- Interrupt control and error detection
- IrDA (SIR mode) encoder and decoder module
- Loop-back mode for test
- Low power mode for Rx path
- Monitor and elimination of Rx baud rate error and own frequency drift automatically for Rx path
- UART Rx timeout mechanism
- DMA interface for DMA transfer
  - DMA as DMA TRx flow controller
  - UART as DMA Rx flow controller
- Operation mode
  - Polling mode
  - Interrupt mode
  - DMA mode

3.20.2 LOGUART

The RTL8711Dx has one LOGUART. LOGUART is responsible for printing logs. It can print logs from four sources at the same time without disordered logs, also it can receive commands for CPU to process.

The LOGUART features:
- Clock source: XTAL40M, OSC2M
- Follows UART protocol
- Various UART format: 1 start bit, 7/8 data bits, 0/1 parity bit and 1/2 stop bits
- Up to 3Mbps baud rate for fast log printing
- Fractional baud rate
- Monitor function to eliminate Rx baud rate error and own frequency drift automatically for Rx path
- Four Tx ports for multi-core or multi-function to print log, which are KM4 CPU, KM0 CPU, Bluetooth, and Bluetooth firmware
- Supports UART relay function, Bluetooth firmware log of UART protocol from other SoC can be relayed by this IP to print out through one Tx port
- Hardware arbitration for Tx ports so that all Tx ports can print log concurrently without disordered log
- Independent open and close for four Tx ports
- Tx AGG supported, hardware adds AGG header automatically so that console can separate logs from different Tx ports
- Wakes up the system when the clock source is open during sleep mode

3.21 Serial Peripheral Interface (SPI0, SPI1)

The RTL8711Dx features up to two SPIs (SPI0, SPI1) that allow communication at up to 50Mbps in master and slave modes, in half-duplex, full-duplex and simplex modes. All SPI interfaces support hardware CRC calculation and 64x16-bit embedded Rx and Tx FIFOs with DMA capability.

The SPI has the following features:
- Supports Motorola SPI Serial interface operation
- Master and slave operation mode
- Provides two high-speed SPI ports: configured as master or slave with max. baud rate 50Mbps
- DMA interface for DMA transfer
- Independent masking of interrupts
- The Transmit and Receive FIFO buffers are 64 words in depth. The FIFO width is fixed at 16 bits.
- Hardware/Software slave-select
  - Dedicated hardware slave-select lines
  - Software control to select target serial-slave device
- Programmable features
  - Clock bit-rate – Dynamic control of the serial bit rate of the data transfer, only when configured in Master Mode.
  - Data frame size (4 to 16 bits) – Frame size of each data transfer under the control of the programmer.
  - Configurable clock polarity and phase
  - Programmable delay sample time of the received serial data bit (rxd), when configured in Master Mode

- Transfer mode
  - Transmit and receive
  - Transmit only
  - Receive only
- Operation mode
  - Polling mode
  - Interrupt mode
  - DMA mode

3.22 Octal Serial Peripheral Interface (OSPI)

The OSPI is an extension of SPI interface. It is used to transmit/receive data from/to SPI slave device, such as a display panel with the OSPI interface. It supports the following features:

- Supports multiple interfaces:
  - SPI
  - Dual SPI
  - Quad SPI
  - Octal SPI
- Programmable features:
  - Clock rate
  - Command
  - Address
  - Data length
  - Data channel number
- Two configurable modes:
  - SDR
  - DDR
- Data/command toggle signal
- Supports multiple serial modes:
  - Mode 0
  - Mode 3
- Interrupt control
- Supports DMA mode

3.23 Light Emitting Diode Controller (LEDC)

The RTL8711Dx embeds a LEDC, which is used to drive external smart LEDs.

The LEDC supports the following features:

- Clock source: XTAL40M
- Configurable LED output high/low level time from 0 to 6.4us
- Configurable LED refresh period up to 400us
- DMA interface with LEDC as DMA flow controller
- Configurable RGB888 display mode
- Maximum 1024 LED serial connection
- Transmit FIFO is 32*24 bits
- Configurable IDLE state output level
- Operation mode
  - DMA mode
  - Interrupt mode

3.24 Infrared Radiation (IR)

The RTL8711Dx embeds one infrared radiation (IR).

The IR is mainly designed to process IR signals with carrier frequency under 500kHz. The hardware IP supports hardware modulation which can be used on the IR Tx transmission. It also can detect the period of a continuous high/low level signal, and record in Rx FIFO, and then the software can recognize a received IR signal serial and process it. IR module works in Half-duplex mode.

It supports the following features:

- Half-duplex mode
  - Tx mode: carrier frequency range is from 25kHz to 500KHz
  - Rx mode: maximum sample frequency is 100MHz
- 32*4 bytes FIFO depth
  - Tx FIFO: Tx carrier symbol count and Tx data state
  - Rx FIFO: Rx data Level and Rx data count
- Customizable carrier duty by users
- Tx Compensation Mechanism
- Optional to modulate space symbol to carrier symbol
- IR receiver front can be IR receiver module or IR diode
- IR Rx glitch filter from 10ns to 90ns
- Operation mode:
  - Interrupt mode
  - Polling mode

3.25 General Purpose Analog-to-Digital Converter (ADC)

The RTL8711Dx integrates a 12-bit successive-approximation register (SAR) ADC, which provides a solution for collecting analog sensor and system power-consumption data with a low-power requirement in itself. Various operation modes, for instance, auto mode, timer-trigger mode, comparator-assist mode, and software-trigger mode, are adopted according to different using strategies.

It has the following features:
- Resolution: 12-bit SAR
- Available channel number
  - 7 external channels and 1 VBAT channel
  - 3 internal channels
- Configurable input
  - Single-ended
  - Differential with predefined channel pair
- Built-in calibration
- Wide input voltage range
- Configurable ADC clock source
- Configurable channel switch order and channel number
- Individual channel compare mode
- Multi-sampling trigger sources
  - Software
  - Timer
- Manual and auto mode conversion
  - Manual mode for software-controllable conversion
  - Auto mode for hardware continuous conversion
- Hardware oversample for higher SNR

3.26 Cap-Touch Controller (CTC)

Self-capacitance touch controller measures the capacitance between the capacitive sensor pin and ground. The capacitive touch controller detects the presence of a finger on or near a touch surface through capacitance changes.

It has the following features:
- 4 capacitive sensor channels:
  - Detection of finger touch
  - Programmable enable/disable for each channel
  - Adjustable sensitivity for each channel
  - Adjustable touch threshold for each channel
- Automatic channel scan: hardware scans each enabled channel automatically in sequence
- Programmable scan period: sample number and scan interval
- Configurable sample clock
- Active noise immunity:
  - Supports SNR information monitor
  - Adjustable environmental noise threshold for each channel
  - Enhanced noise filter for higher SNR
- Automatic environment tracking and calibration (ETC)

  - Automatic hardware baseline initialization
  - Automatic baseline and threshold update for different noise environments
  - Programmable ETC update step and factor
- Programmable button debounce function
- Interrupt control:
  - Programmable interrupt enabled for each interrupt source
  - Software readable interrupt status and raw status register
- Low power consumption

3.27 Key-Scan

As a keypad scan device, the Key-Scan can be applied to simple key, remote control or even game pad. It needs to scan the operations of key press and release accurately and timely.

The major benefit of Key-Scan is to free up the CPU from scanning the keypad all the time. It triggers the corresponding interrupts to inform CPU in time. In addition, the RTL8711Dx can enter low power mode most of time, and take little time to wake up and handle the key events.

It has the following features:
- Up to 8 *8 (64) keypad array with use of 16 GPIOs
- Configurable rows and columns of keypad array
- Hardware debounce with configurable time at each scan
- Configurable Scan Clock, Scan Interval, and Release Time
- Interrupts, interrupts mask, interrupts clear, interrupts status
- Multi-key detect
- FIFO with a width of 12 bits and a depth of 16 to store Key Press and Release Events
- Two work modes: Event (Press and Release) Trigger Mode and Regular Scan Mode (high priority)
- Low power mode: Key press event can wakeup CPU from sleep
- Supports stuck key handling

4 Electrical Characteristics

4.1 Parameters Definitions

4.1.1 Minimum and Maximum Values

Unless otherwise specified, all data are guaranteed by design, simulation and samples test to be applicable to all declared temperature, voltage ranges and processes, and are not tested in production.

4.1.2 Typical Values

Unless otherwise specified, the typical values are reference results when the IC is at an ambient temperature of 25°C and an operating voltage of 3.3V. This value is for reference design only and not actually tested.

4.1.3 Pin Status

4.1.3.1 Loading Capacitor

Unless otherwise specified, the load refers to the equivalent capacitance mounted on the chip pin. Schematic diagram used for loading capacitor measurements is illustrated in *Figure 4-1*.

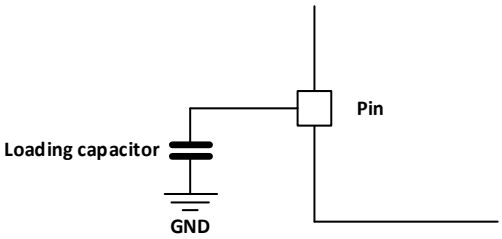


Figure 4-1 Loading capacitor diagram of pin

4.1.3.2 Input Voltage

Unless otherwise specified, the input voltage of the chip pin refers to the voltage difference between the pin and ground. The schematic diagram is illustrated in *Figure 4-2*.

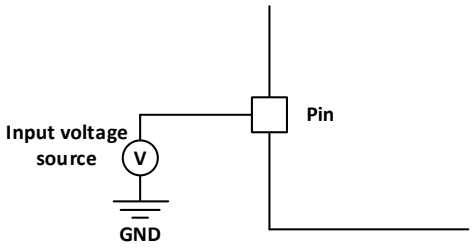


Figure 4-2 Input voltage diagram of pin

4.2 Absolute Maximum Ratings

Stresses beyond absolute maximum ratings may cause permanent damage to the device. These are emphasized ratings only and do not address functional operation of the device.

Table 4-1 Absolute maximum ratings

Symbol	Description	Condition	Min.	Max.	Unit
VAH_DCDC, VAH_LDOM, VDH_IO1, VDH_IO2, VRH_PAD_A, VRH_PA_A, VDH_IO3, VAH_XTAL, VRH_SYN, VDH_RTC, VAH_ADC, VRH_PA_G	The voltage difference between the power pin and GND	Input voltage at power pin	-0.3	3.63	V
BAT_MEAS	The voltage difference between the BAT_MES pin and GND	Input voltage at BAT_MEAS pin	TBD	6.4	V
V_{IN}	The difference between the input voltage on the PA*x*/PB*x* pins and GND	Input DC voltage at digital I/O pin, VDH_IO*x*≤3.63V	-0.3	VDH_IO*x*+0.3	V
P_ANT	Maximum power at receiver	Input RF power at antenna pin		0	dBm
T_{STORE}	Storage temperature range		-65	+150	°C
MSL	Moisture Sensitivity Level			MSL3	
HBM	ESD Human Body Model	T_A=25°C, conforming to JESD22-A114F		Class 2	
CDM	ESD Charged Device Model	T_A=25°C, conforming to JESD22-C101F		Class C2	

4.3 Operation Conditions

Table 4-2 Recommended operation conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
VAH_LDOM, VRH_PAD_A, VRH_PA_A, VRH_PA_G, VRH_SYN, VAH_XTAL, VAH_ADC, VDH_IO3, VAH_DCDC, VDH_RTC[1]	Regular voltage	2.97	3.3	3.63	V
	Wide-range voltage	1.71	1.8/3.3	3.63	V
VDH_IO1, VDH_IO2[2]		1.71	1.8/3.3	3.63	V
LDOM_OUT		1.7	1.8	1.95	V
VRM_RF, VRM_SYN, VAM_AFE, VAM_LDOC	Active mode	1.2	1.25	1.4	V
	Sleep mode	0.65	0.7/0.8	0.85	V
VDL_CORE, LDOC_OUT, VAL_PLL	Active mode	0.85	0.9/1.0	1.05	V
	Sleep mode	0.65	0.7/0.8	0.85	V
T_J	Junction temperature	-40	-	+125	°C

NOTE

[1] All these power pins must be powered by the same voltage. For IC's stable performance, voltage ripple on these pins is suggested to be under +/-100mV.

[2] Power for VDH_IO1 and VDH_IO2 needs to be not higher than power for VAH_LDOM.

4.4 Power Sequence

The recommended power-on and power-off sequences are depicted in the following sections. The VDH_*x*/VAH_*x*/VRH_*x* and CHIP_EN are powered and controlled by external sources. Other used voltages are recommended to be powered by the embedded regulator or LDO.

NOTE

VDH_x/VAH_x/VRH_x refers to power supply including VAH_LDOM, VDH_IO1, VDH_IO2, VRH_PAD_A, VRH_PA_A, VRH_PA_G, VRH_SYN, VAH_XTAL, VAH_ADC, VDH_RTC and VAH_DCDC.

The parameter specification of power sequence is listed in *Table 4-3*.

Table 4-3 Power sequence specification

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{NORMAL}	VDH_*x*/VAH_*x*/VRH_*x* normal operation voltage	Regular voltage	2.97	3.3	3.63	V
		Wide-range voltage	1.71	1.8/3.3	3.63	V
V_{POR_H}	Power on reset high level, release reset threshold	Regular voltage or wide-range voltage	1.9	2.1	2.7	V
		Wide range voltage	0.8	1.2	1.5	V
V_{POR_L}	Power on reset low level	Regular voltage or wide-range voltage	1.0	1.6		V
		Wide range voltage	0.75	1.2		V
V_{IL}	CHIP_EN input low voltage				0.35*V_{NORMAL}	V
V_{IH}	CHIP_EN input high voltage		0.65*V_{NORMAL}			V
T_0	VDH_*x*/VAH_*x*/VRH_*x* rising time		0.1			ms
T_1	VDH_*x*/VAH_*x*/VRH_*x* ready time				3.2	ms
T_2	VDH_*x*/VAH_*x*/VRH_*x* falling time		0.1	100		ms
T_3	VDH_*x*/VAH_*x*/VRH_*x* low voltage last time		0.1			ms
Debounce time	CHIP_EN debounce time, set by registers					ms
T_4	CHIP_EN low voltage last time		0.1			ms

4.4.1 Power-on Sequence

During power on, the VDH_*x*/VAH_*x*/VRH_*x* needs to rise monotonously. When the VDH_*x*/VAH_*x*/VRH_*x* is over V_{POR_H} and the CHIP_EN is high, the IC releases internal reset, and the VDH_*x*/VAH_*x*/VRH_*x* needs to rise up to V_{NORMAL} within T_1. There is no restriction that CHIP_EN is pulled up earlier or later than VDH_*x*/VAH_*x*/VRH_*x* or at the same time with VDH_*x*/VAH_*x*/VRH_*x*. When the power-on parameter T_1 is not within specification, the CHIP_EN can be pulled up later when the VDH_*x*/VAH_*x*/VRH_*x* is up to V_{NORMAL} to avoid related problems caused by this violation.

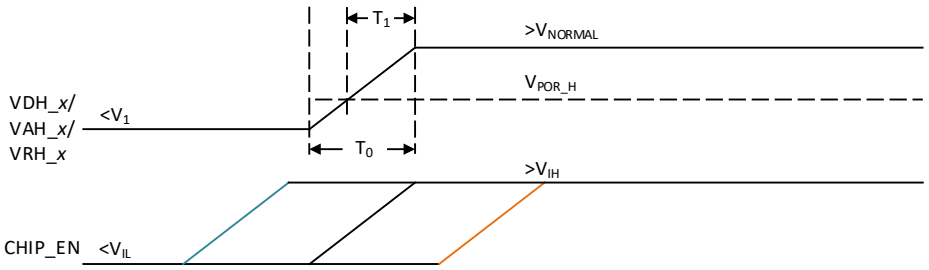


Figure 4-3 Power-on sequence

4.4.2 Power-off Sequence

In the process of power-off, the VDH_*x*/VAH_*x*/VRH_*x* needs to drop down below V_{POR_L} and lasts for at least T_3 before it can be boosted and the IC can be powered on again. Any voltage between 2.7V and V_{POR_L} may not trigger a reset, and it may cause the IC to work abnormally. The watchdog timers or CHIP_EN reset should be used to handle this situation.

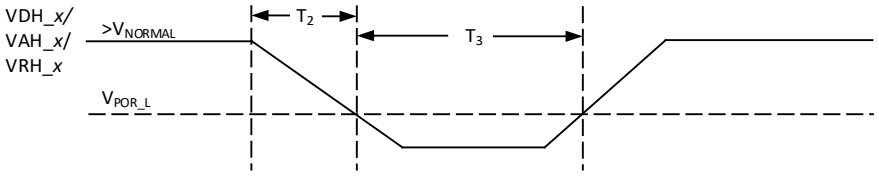


Figure 4-4 Power-off sequence

4.4.3 CHIP_EN Reset Sequence

When using the CHIP_EN as normal reset function, you can set the expected debounce time, ranging from 0us to 16ms. This time may have max. ±50% variation under different conditions, such as different voltage, temperature, etc. When reset, the pull-down time must be T_4 more than debounce time, and the variation of debounce time needs to be taken into consideration.

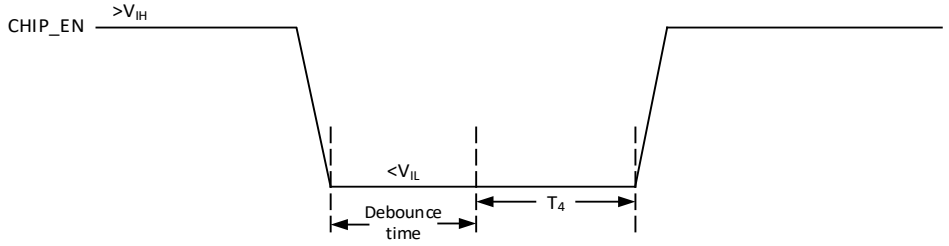


Figure 4-5 CHIP_EN reset sequence

4.5 Reset Detection

The parameters given in *Table 4-4* are derived from the test under ambient operating temperature.

Table 4-4 Embedded power supply supervisor characteristics

Symbol	Parameter	Configuration	Min.	Typ.	Max.	Unit
V_{BOD_L} & V_{BOD_H}	Brownout detect threshold	BOD_THRESHOLD1	-5%	2.85	+5%	V
		BOD_THRESHOLD2		2.82		V
		BOD_THRESHOLD3		2.78		V
		BOD_THRESHOLD4		2.74		V
		BOD_THRESHOLD5		2.7		V
		BOD_THRESHOLD6		2.65		V
		BOD_THRESHOLD7		2.61		V
		BOD_THRESHOLD8		2.57		V
		BOD_THRESHOLD9		2.53		V
		BOD_THRESHOLD10		2.49		V
		BOD_THRESHOLD11		2.45		V
		BOD_THRESHOLD12		2.41		V
		BOD_THRESHOLD13		2.37		V
		BOD_THRESHOLD14		2.33		V
		BOD_THRESHOLD15		2.21		V
		BOD_THRESHOLD16		2.17		V
		BOD_THRESHOLD17		2.12		V
		BOD_THRESHOLD18		2.08		V
		BOD_THRESHOLD19		2.04		V
		BOD_THRESHOLD20		2		V
		BOD_THRESHOLD21		1.96		V
		BOD_THRESHOLD22		1.93		V
		BOD_THRESHOLD23		1.88		V
		BOD_THRESHOLD24		1.84		V
		BOD_THRESHOLD25		1.8		V
		BOD_THRESHOLD26		1.76		V
		BOD_THRESHOLD27		1.72		V
		BOD_THRESHOLD28		1.69		V
		BOD_THRESHOLD29		1.65		V
		BOD_THRESHOLD30		1.62		V
		BOD_THRESHOLD31		1.59		V

NOTE

The V_{BOD_L} and V_{BOD_H} can be set independently, and V_{BOD_H} needs to be set higher than V_{BOD_L}. It is recommended to reserve about 200mV or higher hysteresis window between V_{BOD_H} and V_{BOD_L}.

4.6 Embedded Regulators Characteristics

The characteristics of embedded regulators including LDOC, DCDC, and LDOM are guaranteed by design.

Table 4-5 Embedded regulators characteristics

Regulators	Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
LDOC	V_{IN}	Input voltage range	LDO mode	1.20	1.25/1.35	1.45	V
			Bypass mode	0.6	0.7	0.9	
	V_{OUT}	Output voltage range	LDO mode	0.81	0.9/1.0	1.05	V
DCDC	V_{IN}	Input voltage range		1.71	1.8/3.3	3.63	V
	V_{OUT}	Output voltage range		0.6	1.25/1.35	1.45	V
	F	Switching frequency	PWM mode	-	2	-	MHz
LDOM	V_{IN}	Input voltage range		1.71	3.3	3.63	V
	V_{OUT}	Output voltage range		1.7	1.8	1.9	V

4.7 Crystal Characteristics

The RTL8711Dx has a built-in 40MHz crystal oscillation circuit to provide a stable, controllable system clock. With the built-in capacitor, the frequency offset can be fine-tuned.

The characteristic requirements of external crystal are listed in *Table 4-6*.

Table 4-6 Characteristic requirements of external crystal

Parameters	Min.	Typ.	Max.	Unit
Frequency		40		MHz
Frequency stability	-10		10	ppm
Frequency make tolerance	-10		10	ppm
Supported driving level	100			µW
ESR			40	Ω
Load capacitance CL			9	pF
Shunt capacitance Co			2	pF

4.8 Power Consumption Characteristics (TBD)

The power consumption data is the result of the IC powered by 3.3V or 1.8V at different ambient temperatures. The power consumption is affected by process deviation, temperature, and voltage.

The IC is under the following working conditions:

- Except for LOGUART Tx/Rx (PB5/PB4), other I/O pins are in input mode.
- All peripherals except GPIOs are disabled.

4.9 I/O Pin Characteristics

This section applies when GPIO is used as a digital function, but not used as an analog function.

Table 4-7 Output/input voltage level of I/O ports

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{IL}	I/O input low level voltage	V_{IO}[1]=1.8V±10%	-0.3	-	0.35*V_{IO}	V
		V_{IO}=3.3V±10%	-0.3	-	0.8	
V_{IH}	I/O input high level voltage	V_{IO}=1.8V±10%	0.65* V_{IO}	-	-	
		V_{IO}=3.3V±10%	2	-	-	
V_{OL}	I/O output Low level voltage	V_{IO}=1.8V±10%	-	-	0.15*V_{IO}	
		V_{IO}=3.3V±10%	-	-	0.15*V_{IO}	
V_{OH}	I/O output high level voltage	V_{IO}=1.8V±10%	0.85*V_{IO}	-	-	
		V_{IO}=3.3V±10%	0.85*V_{IO}	-	-	

NOTE

[1] V_{IO} is the power supply for I/O pin.

Table 4-8 Driving strength and pull up/down resistors of I/O port working at 1.8V[1]

Pin name	Driving strength (mA)[2]			Internal pull resistor (ohm)			Resistor available in deep-sleep mode?
	Min.	Typ.	Max.	Min.	Typ.	Max.	
PA6~PA11	4/8[3]	-	-	TBD	160k[4]	TBD	Yes
PA12	2/4	-	-	TBD	160k	TBD	Yes
PA13~PA18	4/8	-	-	TBD	160k	TBD	Yes
PA19~PA25	4/8	-	-	TBD	9.4k/50k[5]	TBD	Yes
PA28~PA29	2/4	-	-	TBD	PU:4.4k/50k PD:43k	TBD	Yes
PA26~PA27, PA30~PB3	4/8	-	-	TBD	4.7k/50k	TBD	Yes
PB4~PB12	4/8	-	-	TBD	9.4k/50k	TBD	Yes
PB13~PB28	2/4	-	-	TBD	160k	TBD	Yes
PB30~PB31	4/8	-	-	TBD	160k	TBD	Yes

NOTE

[1] The data in this table applies to all I/O ports operating at 1.8V (±10%).

[2] The driving capability is obtained by measuring the sinking current or sourcing current when the I/O port output high or low by using a voltage source on the I/O port to fix the port voltage level to $V_{OH(min.)}$ or $V_{OL(max.)}$.

[3] Both sinking and sourcing currents conform to the data in the table.

[4] Except for PA28~PA29, the pull-up and pull-down resistors' values of each I/O port are the same.

[5] When there are two values in the Typ. column, it means that the I/O port has two levels of resistors to choose from.

Table 4-9 Driving strength and pull up/down resistors of I/O port working at 3.3V[1]

Pin name	Driving strength (mA)[2]			Internal pull resistor (ohm)			Resistor available in deep sleep mode?
	Min.	Typ.	Max.	Min.	Typ.[5]	Max.	
PA6~PA11	8/16[3]	-	-	TBD	80k[4]	TBD	Yes
PA12	4/8	-	-	TBD	80k	TBD	Yes
PA13~PA18	8/16	-	-	TBD	80k	TBD	Yes
PA19~PA25	8/16	-	-	TBD	4.7k/50k	TBD	Yes
PA28~PA29	4/8	-	-	TBD	PU:2.2k/50k PD:21.5k	TBD	Yes
PA26~PA27, PA30~PB3	8/16	-	-	TBD	4.7k/50k	TBD	Yes
PB4~PB12	8/16	-	-	TBD	4.7k/50k	TBD	Yes
PB13~PB28	4/8	-	-	TBD	80k	TBD	Yes
PB30~PB31	8/16	-	-	TBD	80k	TBD	Yes

NOTE

[1] The data in this table applies to all I/O ports operating at 3.3V (±10%).

[2] The driving capability is obtained by measuring the sinking current or sourcing current when the I/O port output high or low by using a voltage source on the I/O port to fix the port voltage level to $V_{OH(min.)}$ or $V_{OL(max.)}$.

[3] Both sinking and sourcing currents conform to the data in the table.

[4] Except for PA28~PA29, the pull-up and pull-down resistors' values of each I/O port are the same.

[5] When there are two values in the Typ. column, it means that the I/O port has two levels of resistors to choose from.

4.10 RF Characteristics

4.10.1 WLAN Radio Specifications

This section describes the RF characteristics of WLAN 2.4GHz and 5GHz radios. Unless otherwise defined, all these values are provided at the antenna port with the front-end loss.

4.10.1.1 WLAN 2.4GHz Band Receiver Performance

Table 4-10 WLAN 2.4GHz band receiver performance

Parameter	Condition	Performance (3.3V)			Performance (1.8V)			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Frequency Range	Center channel frequency	2412		2484	2412		2484	MHz
Rx Sensitivity 802.11b	1Mbps CCK		-100			-100		dBm
	2Mbps CCK		-97			-97		dBm
	5.5Mbps CCK		-94			-94		dBm
	11Mbps CCK		-90.5			-90.5		dBm
Rx Sensitivity 802.11g	BPSK rate 1/2, 6Mbps OFDM		-95			-95.5		dBm
	BPSK rate 3/4, 9Mbps OFDM		-93.5			-94		dBm
	QPSK rate 1/2, 12Mbps OFDM		-92.5			-93		dBm
	QPSK rate 3/4, 18Mbps OFDM		-90.5			-90.5		dBm
	16-QAM rate 1/2, 24Mbps OFDM		-87			-87.5		dBm
	16-QAM rate 3/4, 36Mbps OFDM		-84			-84		dBm
	64-QAM rate 1/2, 48Mbps OFDM		-79.5			-80		dBm
	64-QAM rate 3/4, 54Mbps OFDM		-78			-78.5		dBm
Rx Sensitivity 802.11n BW = 20MHz Mixed Mode 800ns Guard Interval Non-STBC	MCS 0, BPSK rate 1/2		-95			-95		dBm
	MCS 1, QPSK rate 1/2		-92			-92.5		dBm
	MCS 2, QPSK rate 3/4		-90			-90		dBm
	MCS 3, 16-QAM rate 1/2		-87			-87		dBm
	MCS 4, 16-QAM rate 3/4		-83.5			-83.5		dBm
	MCS 5, 64-QAM rate 2/3		-79			-79.5		dBm
	MCS 6, 64-QAM rate 3/4		-77.5			-78		dBm
	MCS 7, 64-QAM rate 5/6		-76			-76.5		dBm
Rx Sensitivity 802.11n BW = 40MHz Mixed Mode 800ns Guard Interval Non-STBC	MCS 0, BPSK rate 1/2		-92			-92		dBm
	MCS 1, QPSK rate 1/2		-89			-89		dBm
	MCS 2, QPSK rate 3/4		-87			-87		dBm
	MCS 3, 16-QAM rate 1/2		-83.5			-83.5		dBm
	MCS 4, 16-QAM rate 3/4		-80.5			-80.5		dBm
	MCS 5, 64-QAM rate 2/3		-75.5			-75.5		dBm
	MCS 6, 64-QAM rate 3/4		-74			-74.5		dBm
	MCS 7, 64-QAM rate 5/6		-73			-73		dBm
Max. Receive Level	6Mbps OFDM		0			0		dBm
	54Mbps OFDM		0			0		dBm
	11n, MCS 0, HT20		0			0		dBm
	11n, MCS 7, HT20		0			0		dBm
	11n, MCS 0, HT40		0			0		dBm
	11n, MCS 7, HT40		0			0		dBm
Adjacent Channel Rejection	11Mbps CCK		43			43		dB
	BPSK rate 1/2, 6Mbps OFDM		44			44		dB
	64-QAM rate 3/4, 54Mbps OFDM		26			26		dB
	HT20, MCS 0, BPSK rate 1/2		43			43		dB
	HT20, MCS 7, 64-QAM rate 5/6		23			23		dB
	HT40, MCS 0, BPSK rate 1/2		32			32		dB
	HT40, MCS 7, 64-QAM rate 5/6		14			14		dB

4.10.1.2 WLAN 2.4GHz Band Transmitter Performance

Table 4-11 WLAN 2.4GHz band transmitter performance

Parameter	Condition	Performance (3.3V)			Performance (1.8V)			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Frequency Range	Center channel frequency	2412		2484				MHz
Output power with spectral mask and EVM compliance[1]	1Mbps CCK		20			15		dBm
	11Mbps CCK		20			15		dBm
	BPSK rate 1/2, 6Mbps OFDM		19			14		dBm
	64-QAM rate 3/4, 54Mbps OFDM		18			12		dBm
	HT20, MCS 0, BPSK rate 1/2		19			14		dBm
	HT20, MCS 7, 64-QAM rate 5/6		17			11		dBm
	HT40, MCS 0, BPSK rate 1/2		19			14		dBm
	HT40, MCS 7, 64-QAM rate 5/6		17			11		dBm
Tx EVM	BPSK rate 1/2, 6Mbps OFDM		-30	-5		-28	-5	dB

	64-QAM rate 3/4, 54Mbps OFDM		-34	-25		-34	-25	dB
	HT20, MCS 0, BPSK rate 1/2		-30	-5		-28	-5	dB
	HT20, MCS 7, 64QAM rate 5/6		-34	-27		-34	-27	dB
	HT40, MCS 0, BPSK rate 1/2		-29	-5		-26	-5	dB
	HT40, MCS 7, 64-QAM rate 5/6		-33	-27		-32	-27	dB
Output power variation	After do power trim at FT	-1.5		1.5	-1.5		1.5	dB
Carrier suppression			-40	-30		-40	-30	dBc
Harmonic output power[2]	2nd harmonic		-18			-25		dBm/MHz
	3rd harmonic		-22			-25		dBm/MHz
Harmonic output power[3]	2nd harmonic			-50			-50	dBm/MHz
	3rd harmonic			-50			-50	dBm/MHz

NOTE

[1] Power level is tested after Digital Pre-Distortion (DPD) enable.

[2] Harmonic output power is tested at IC port.

[3] Harmonic output power is measured at RF connector with diplexer (RFDIP1606LB598D1T) and appropriate matching.

4.10.1.3 WLAN 5GHz Band Receiver Performance

Table 4-12 WLAN 5GHz band receiver performance

Parameter	**Condition**	**Performance (3.3V)**			**Performance (1.8V)**			**Unit**
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Frequency Range	Center channel frequency	5180		5825	5180		5825	MHz
Rx Sensitivity 802.11a	BPSK rate 1/2, 6Mbps OFDM		-94.5			-94.5		dBm
	BPSK rate 3/4, 9Mbps OFDM		-92.5			-93		dBm
	QPSK rate 1/2, 12Mbps OFDM		-91.5			-92		dBm
	QPSK rate 3/4, 18Mbps OFDM		-89.5			-89.5		dBm
	16-QAM rate 1/2, 24Mbps OFDM		-86.5			-86.5		dBm
	16-QAM rate 3/4, 36Mbps OFDM		-83			-83		dBm
	64-QAM rate 1/2, 48Mbps OFDM		-78.5			-79		dBm
	64-QAM rate 3/4, 54Mbps OFDM		-77			-77		dBm
Rx Sensitivity 802.11n BW = 20MHz Mixed Mode 800ns Guard Interval Non-STBC	MCS 0, BPSK rate 1/2		-94			-94		dBm
	MCS 1, QPSK rate 1/2		-91.5			-91.5		dBm
	MCS 2, QPSK rate 3/4		-89			-89		dBm
	MCS 3, 16-QAM rate 1/2		-86			-86		dBm
	MCS 4, 16-QAM rate 3/4		-82.5			-82.5		dBm
	MCS 5, 64-QAM rate 2/3		-78			-78		dBm
	MCS 6, 64-QAM rate 3/4		-76.5			-76.5		dBm
	MCS 7, 64-QAM rate 5/6		-75			-75		dBm
Rx Sensitivity 802.11n BW = 40MHz Mixed Mode 800ns Guard Interval Non-STBC	MCS 0, BPSK rate 1/2		-91			-91		dBm
	MCS 1, QPSK rate 1/2		-88.5			-88		dBm
	MCS 2, QPSK rate 3/4		-85.5			-85.5		dBm
	MCS 3, 16-QAM rate 1/2		-82.5			-82.5		dBm
	MCS 4, 16-QAM rate 3/4		-79			-79.5		dBm
	MCS 5, 64-QAM rate 2/3		-74.5			-74.5		dBm
	MCS 6, 64-QAM rate 3/4		-73			-73		dBm
	MCS 7, 64-QAM rate 5/6		-71.5			-71.5		dBm
Max. Receive Level	6Mbps OFDM		0			0		dBm
	54Mbps OFDM		0			0		dBm
	11n, MCS 0, HT20		0			0		dBm
	11n, MCS 7, HT20		0			0		dBm
	11n, MCS 0, HT40		0			0		dBm
	11n, MCS 7, HT40		0			0		dBm
Adjacent Channel Rejection	BPSK rate 1/2, 6Mbps OFDM		33			33		dB
	64-QAM rate 3/4, 54Mbps OFDM		10			10		dB
	HT20, MCS 0, BPSK rate 1/2		29			29		dB
	HT20, MCS 7, 64-QAM rate 5/6		10			10		dB
	HT40, MCS 0, BPSK rate 1/2		29			29		dB
	HT40, MCS 7, 64-QAM rate 5/6		11			11		dB

4.10.1.4 WLAN 5GHz Band Transmitter Performance

Table 4-13 WLAN 5GHz band transmitter performance

Parameter	Condition	Performance (3.3V)			Performance (1.8V)			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Frequency Range	Center channel frequency	5180		5825	5180		5825	MHz
Output power with spectral mask and EVM compliance[1]	BPSK rate 1/2, 6Mbps OFDM		18			12		dBm
	64-QAM rate 3/4, 54Mbps OFDM		16			9		dBm
	HT20, MCS 0, BPSK rate 1/2		18			12		dBm
	HT20, MCS 7, 64-QAM rate 5/6		15			8		dBm
	HT40, MCS 0, BPSK rate 1/2		18			12		dBm
	HT40, MCS 7, 64-QAM rate 5/6		15			8		dBm
Tx EVM	BPSK rate 1/2, 6Mbps OFDM		-30	-5		-28	-5	dB
	64-QAM rate 3/4, 54Mbps OFDM		-32	-25		-32	-25	dB
	HT20, MCS 0, BPSK rate 1/2		-30	-5		-28	-5	dB
	HT20, MCS 7, 64QAM rate 5/6		-33	-27		-33	-27	dB
	HT40, MCS 0, BPSK rate 1/2		-30	-5		-25	-5	dB
	HT40, MCS 7, 64-QAM rate 5/6		-32	-27		-31	-27	dB
Output power variation	After do power trim at FT	-1.5		1.5	-1.5		1.5	dB
Carrier suppression			-40	-30		-40	-30	dBc
Harmonic output power[2]	2nd harmonic		-28			-38		dBm/MHz
	3rd harmonic		-30			-38		dBm/MHz
Harmonic output power[3]	2nd harmonic			-50			-50	dBm/MHz
	3nd harmonic			-50			-50	dBm/MHz

NOTE

[1] Power level is tested after Digital Pre-Distortion (DPD) enable.
[2] Harmonic output power is tested at IC port.
[3] Harmonic output power is measured at RF connector with diplexer (RFDIP1606LB598D1T) and appropriate matching.

4.10.2 Bluetooth Radio Specifications

This section describes the RF characteristics of Bluetooth 2.4GHz radio. Unless otherwise defined, all these values are provided at the antenna port with the front-end loss.

4.10.2.1 Bluetooth Low Energy (BLE) Receiver Performance

Table 4-14 BLE receiver performance

Parameter	Condition	Performance (3.3V)			Performance (1.8V)			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Frequency Range	Center channel frequency	2402		2480	2402		2480	MHz
Receiver Sensitivity	PER<30.8%	-99			-99			dBm
Max. Usable Signal	PER<30.8%	0			0			dBm
C/I co-channel (PER<30.8%)	Co-channel sensitivity		5			5		dB
C/I 1MHz (PER<30.8%)	Adjacent channel selectivity		-7			-7		dB
C/I 2MHz (PER<30.8%)	2nd adjacent channel selectivity		-50			-50		dB
C/I >= 3MHz (PER<30.8%)	3rd adjacent channel selectivity		-57			-57		dB
C/I Image Channel (PER<30.8%)	Image channel selectivity		-27			-27		dB
C/I Image 1MHz (PER<30.8%)	1MHz adjacent to image channel selectivity		-28			-28		dB
Inter-modulation		-30			-30			dBm
Out-of-band blocking	30MHz to 2000MHz	-35			-35			dBm
	2003MHz to 2399MHz	-35			-35			dBm
	2484MHz to 2997MHz	-30			-30			dBm
	3000MHz to 12.75GHz	-30			-30			dBm

4.10.2.2 Bluetooth Low Energy (BLE) Transmitter Performance

Table 4-15 BLE transmitter performance

Parameter	Condition	Performance (3.3V)			Performance (1.8V)			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Frequency Range	Center channel frequency	2402		2480	2402		2480	MHz
Output Power	At max. power output level		8			7		dBm
Carrier Frequency Offset and Drift	Frequency offset		±10			±10		kHz
	Frequency drift		±10			±10		kHz
	Max. drift rate		±10			±10		kHz
Modulation characteristics	Δf1 avg.		250			250		kHz
	Δf2 max.		215			210		kHz
	Δf1 avg./Δf2 avg.		0.92			0.92		
In-Band Emissions	±2MHz offset		-51			-51		dBm
	≥ ±3MHz offset		-54			-54		dBm

4.11 General Purpose ADC Characteristics

Table 4-16 ADC characteristics

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
fs	ADC sample frequency			-	-	250	kHz
V_{IN}[1]	Conversion input voltage range	External channel (CH0 ~ CH6)		0	-	Min(3.3, VAH_ADC)	V
		BAT_MEAS		0	-	5.4	
R	Input impedance	External channel (CH0 ~ CH6)		520	-	550	kΩ
		BAT_MEAS		-	156	-	
t_{STAB}	ADC total power-up time	Including internal BG/LDO/ADC power-up time		-	460	-	µs
I_{DDA}	ADC quiescent current	VAH_ADC = 2.7V ~ 3.63V, including internal BG/LDO/ADC		-	302	-	µA
Resolution				-	12	-	bits
EO	Offset error	fs = 166.67kHz VAH_ADC = 3.3V T_A = 25°C	Single-ended			±8	LSB
			Differential			-	
EG	Gain error		Single-ended			±8	
			Differential			-	
INL	Integral linearity error		Single-ended			±8	
			Differential			-	
DNL	Differential linearity error		Single-ended			±2	
			Differential			-	
SFDR	Spurious free dynamic range		Single-ended		58		dB
			Differential		-		
THD	Total harmonic distortion		Single-ended		-50		
			Differential		-		
SNR[2]	Signal-to-noise ratio		Single-ended	62			
			Differential	-			
ENOB[2]	Effective number of bits		Single-ended	10			bits
			Differential	-			

NOTE

[1] Conversion input voltage range: 0 ~ 3.3V (if VAH_ADC >= 3.3V) or 0 ~ VAH_ADC (if VAH_ADC < 3.3V).

[2] There is the ADC performance without calibration which does not include harmonic distortion.

[3] Non-linearity will be corrected after calibration.

4.12 USB Interface Characteristics

The Universal Serial Bus (USB) interface complies with USB 2.0 standard, and supports full speed only. The full-speed data rate is nominally 12.000Mb/s. The following sections gives a brief overview of the electrical requirements on a USB interface. For extensive information, refer to the USB specification.

4.12.1 Signaling Level

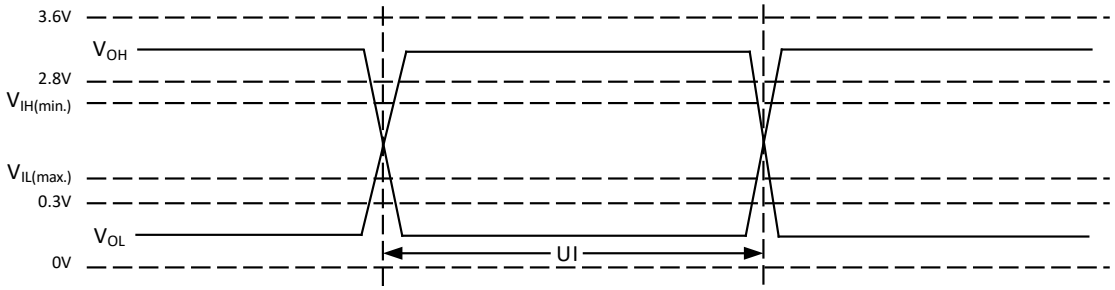


Figure 4-6 Full-speed signal waveforms

Table 4-17 Full-speed signal waveforms parameters

Symbol	Parameter	Conditions	3.3V (2.97V~3.63V)		Unit
			Min.	Max.	
V_{OL}	Output low voltage	Full speed	0	0.3	V
V_{OH}	Output high voltage	Full speed	2.8	3.6	V
UI	Bit period	Full speed	-	83	ns
V_{IL}	Input low voltage	Full speed	-	0.8	V
V_{IH}	Input high voltage	Full speed	2.0	-	V

4.12.2 Signal Rising and Falling Time

The rising and falling time is measured from 10% ~ 90% of the signal low and high levels.

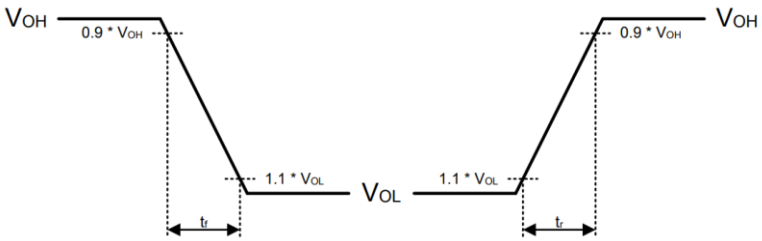


Figure 4-7 Data signal rising and falling time

Table 4-18 Data signal rising and falling time parameter

Symbol	Parameter	Conditions	3.3V (2.97V~3.63V)		Unit
			Min.	Max.	
t_r	Rising/falling time (10% ~ 90%)	Full speed	4	20	ns

4.12.3 Speed Identification

A USB device must identify its data rate capabilities to the USB host. To do this, the USB standard has set up a scheme where USB hosts have a weak pull-down resistor on both data lines, and the devices have a strong pull-up resistor on one of the data lines. The size of these resistors are set to ensure that the pull-up on the device-end will pull the data line from 0V to high (3.0V ~ 3.6V) as seen from the host.

Nominal values for these resistors are 1.5kΩ for the pull-up on the device-end. When a device is connected to a host, the host checks which of the data lines is pulled high.

4.13 UART Characteristics

All measurements are tested under the following conditions:

- The I/O ports are configured with high driving strength.

NOTE

Refer to section 4.9 for the definitions of $V_{OH(min.)}$, $V_{OL(max.)}$, $V_{IH(min.)}$, and $V_{IL(max.)}$.

Table 4-19 Timing data of UART

Item	Conditions	Min.	Typ.	Max.	Unit
Transfer rate	TXD Clock Source: 40MHz XTAL			8000000	bps
	RXD Clock Source: 40MHz XTAL			8000000	bps
	RXD Clock Source: 2MHz OSC			115200	bps

NOTE

Total baud rate error shall be less than 3% in order to communicate correctly, which includes three parts: the error of real baud rate of Tx device and expected communication baud rate, the frequency drift of Rx IP clock, and the calculation baud error of Rx device. Users can enable the function of monitoring baud rate of Rx data to decrease the baud rate error.

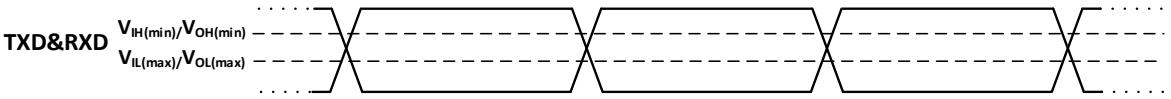


Figure 4-8 Timing diagram of UART

4.14 QSPI Flash Memory Controller Characteristics

This section describes the timing characteristics of the Quad Serial Peripheral Interface (QSPI) for Flash memory controller.

All measurements are tested under the following conditions:

- The maximum loading is 15pF.
- The I/O ports are configured with high driving strength.

Table 4-20 Timing data

Symbol	Parameter	Conditions	Min.	Max.	Unit
T_{SCL}	Clock period	Master	8	-	ns
t_{LOW}	Clock Low Time	Master	45%*TSCL	55%*TSCL	ns
t_{HIGH}	Clock High Time	Master	45%*TSCL	55%*TSCL	ns
t_r	Data/Clock raise time	Master	-	1	ns
t_f	Data/Clock fall time	Master	-	1	ns
$t_{SU;DAT(I)}$	Data input setup time	Master	2	-	ns
$t_{HD;DAT(I)}$	Data input hold time	Master	1	-	ns
$t_{SU;DAT(O)}$	Data output setup time	Master	(TSCL/2)-1	-	ns
$t_{HD;DAT(O)}$	Data output hold time	Master	(TSCL/2)-1	-	ns
$t_{VD;DAT(O)}$	Data output valid time	Master	-1	1	ns
$t_{SU;CS(A)}$	CS active setup time relative to CLK	Master	(TSCL/2)-1	-	ns
$t_{HD;CS(A)}$	CS active hold time relative to CLK	Master	TSCL-1	-	ns

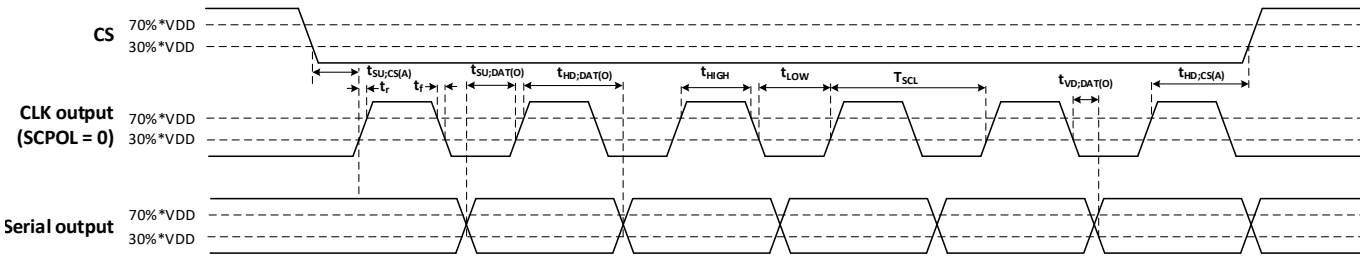


Figure 4-9 Output timing diagram (SCPH = 0)

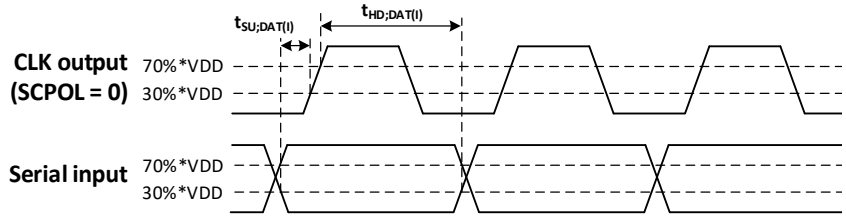


Figure 4-10 Input timing diagram (SCPH = 0)

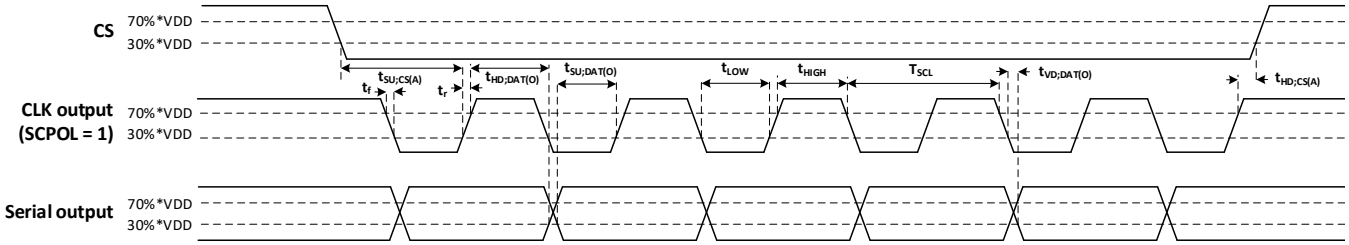


Figure 4-11 Output timing diagram (SCPH = 1)

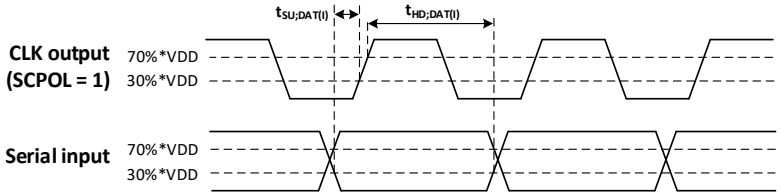


Figure 4-12 Input timing diagram (SCPH = 1)

4.15 SPI Characteristics

The SPI function of RTL8711Dx is divided into dedicated SPI and full-matrix SPI, refer to *Alternate Functions* for the function comparison between them.

The dedicated SPI has the following features:

- Limited choices with fixed group usage, that is to say, only the specified pins configured as function ID8 can be used in combination:
  - Group1 (PA14, PA15, PA16, PA17)
  - Group2 (PA12, PA26, PA27, PA28)
  - Group3 (PB23, PB24, PB25, PB26)
  - Group4 (PA29, PA30, PA31, PB17)
  - Group5 (PB18, PB19, PB20, PB21)
- Better timing performance compared to full matrix SPI.

The full-matrix SPI has the following features:

- More combinations and each pin signal can be flexibly configured, that is to say, more pins that can be freely configured as individual signals of SPI function ID (ID29 (SPI1_CLK), ID30 (SPI1_MISO), ID31 (SPI1_MOSI), ID32 (SPI1_CS)), and can be used in any combination.
- Limited timing performance.

All measurements are tested under the following conditions:

- The maximum loading is 15pF.
- The I/O ports are configured with high driving strength.

NOTE

Refer to section 4.9 for definitions of $V_{OH(min.)}$, $V_{OL(max.)}$, $V_{IH(min.)}$ and $V_{IL(max.)}$.

Table 4-21 Timing data of dedicated SPI

Symbol	Parameter	Conditions	3.3V I/O (2.97V~3.6V)		1.8V I/O (1.71V~1.89V)		Unit
			Min.	Max.	Min.	Max.	
T_{SCL}	SPI clock period	Master	20	-	20	-	ns
		Slave	40	-	40	-	ns
Duty cycle	SPI duty cycle	Master	45	55	45	55	%

		Slave	30	70	30	70	%
$t_{su;CS(M)}/t_{su;CS(S)}$	CS setup time	Master	1.5*T_{SCL} -2	-	1.5* T_{SCL} -2	-	ns
		Slave	15	-	15	-	ns
$t_{HD;CS(M)}/t_{HD;CS(S)}$	CS hold time	Master	T_{SCL} -2	-	T_{SCL} -2	-	ns
		Slave	18	-	18	-	ns
$t_{AC;DAT(MO)}/t_{AC;DAT(SO)}$	Data output access time	Master	T_{SCL} -2	-	T_{SCL} -2	-	ns
		Slave	-	11	-	18	
$t_{VD;DAT(MO)}/t_{VD;DAT(SO)}$	Data output valid time	Master	-2	2	-2	2	ns
		Slave	-	11	-	18	
$t_{SU;DAT(MI)}/t_{SU;DAT(SI)}$	Data input setup time	Master	4	-	4	-	ns
		Slave	2	-	2	-	
$t_{HD;DAT(MI)}/t_{HD;DAT(SI)}$	Data input hold time	Master	2	-	2	-	ns

NOTE

- *The maximum value of $t_{VD;DAT(SO)}$ is already greater than half of a clock cycle, so when used as a slave, the maximum speed supported by SPI is 25MHz. But if the connected master supports sampling delay function, it could support up to 50MHz.*
- *The timing data of $t_{SU;DAT(MI)}$ is only applicable to speeds of 25MHz or below. When the RTL8711Dx is used as a master running at 50MHz, due to the sample delay function of IC, the accepted minimum value of $t_{SU;DAT(MI)}$ can be -16ns.*

Table 4-22 Timing data of full-matrix SPI

Symbol	**Parameter**	**Conditions**	**3.3V I/O (2.97V~3.6V)**		**1.8V I/O (1.71V~1.89V)**		**Unit**
			Min.	Max.	Min.	Max.	
T_{SCL}	SPI clock period	Master	40	-	40	-	ns
		Slave	80	-	80	-	ns
Duty cycle	SPI duty cycle	Master	45	55	45	55	%
		Slave	30	70	30	70	%
$t_{su;CS(M)}/t_{su;CS(S)}$	CS setup time	Master	1.5*T_{SCL} -4	-	1.5* T_{SCL} -6	-	ns
		Slave	15	-	15	-	ns
$t_{HD;CS(M)}/t_{HD;CS(S)}$	CS hold time	Master	T_{SCL} -4	-	T_{SCL} -6	-	ns
		Slave	18	-	18	-	ns
$t_{AC;DAT(MO)}/t_{AC;DAT(SO)}$	Data output access time	Master	T_{SCL} -4	-	T_{SCL} -6	-	ns
		Slave	-	15	-	22	
$t_{VD;DAT(MO)}/t_{VD;DAT(SO)}$	Data output valid time	Master	-4	4	-7	7	ns
		Slave	-	18	-	24	
$t_{SU;DAT(MI)}/t_{SU;DAT(SI)}$	Data input setup time	Master	4	-	4	-	ns
		Slave	2	-	2	-	
$t_{HD;DAT(MI)}/t_{HD;DAT(SI)}$	Data input hold time	Master	2	-	2	-	ns
		Slave	1	-	1	-	

NOTE

If the connected master supports sampling with a delay, the SPI slave could support up to 25MHz.

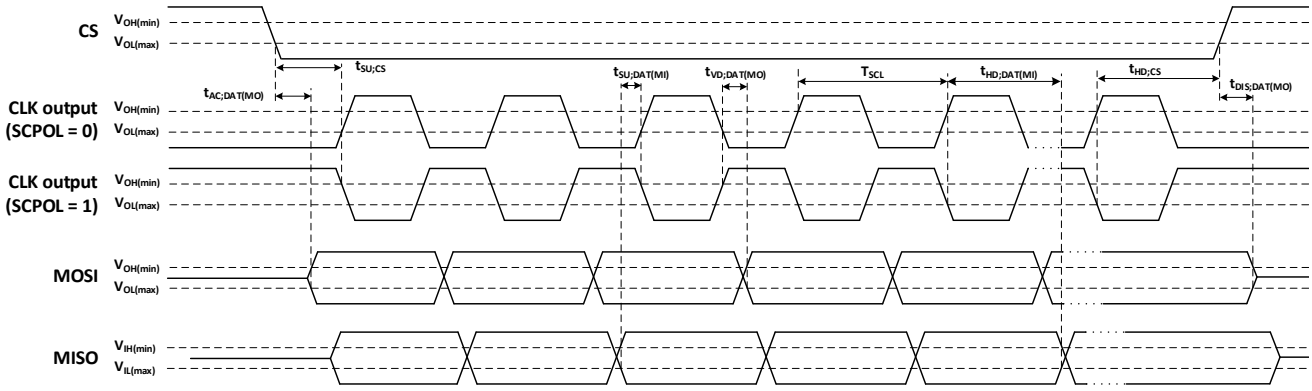


Figure 4-13 Timing diagram for master (SCPH = 0)

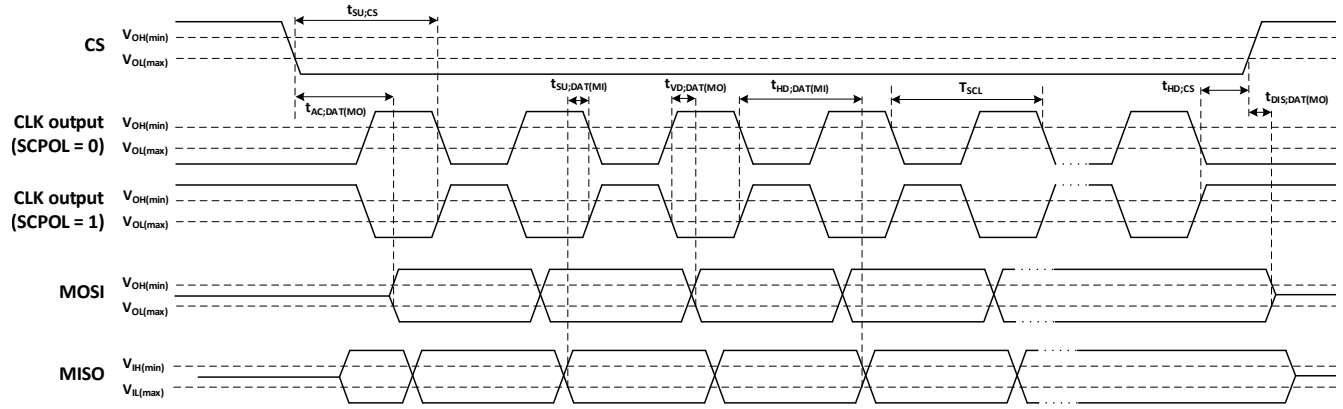


Figure 4-14 Timing diagram for master (SCPH = 1)

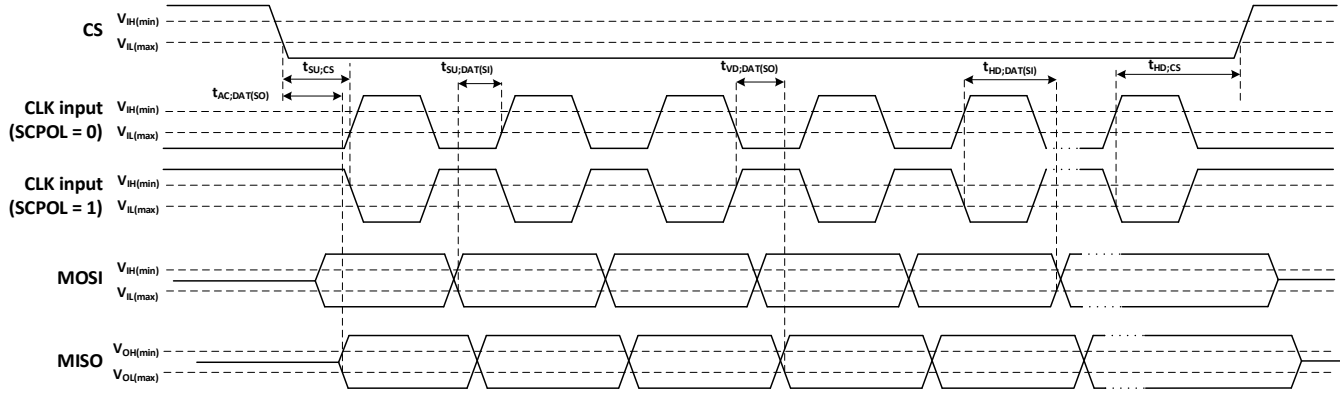


Figure 4-15 Timing diagram for slave (SCPH = 0)

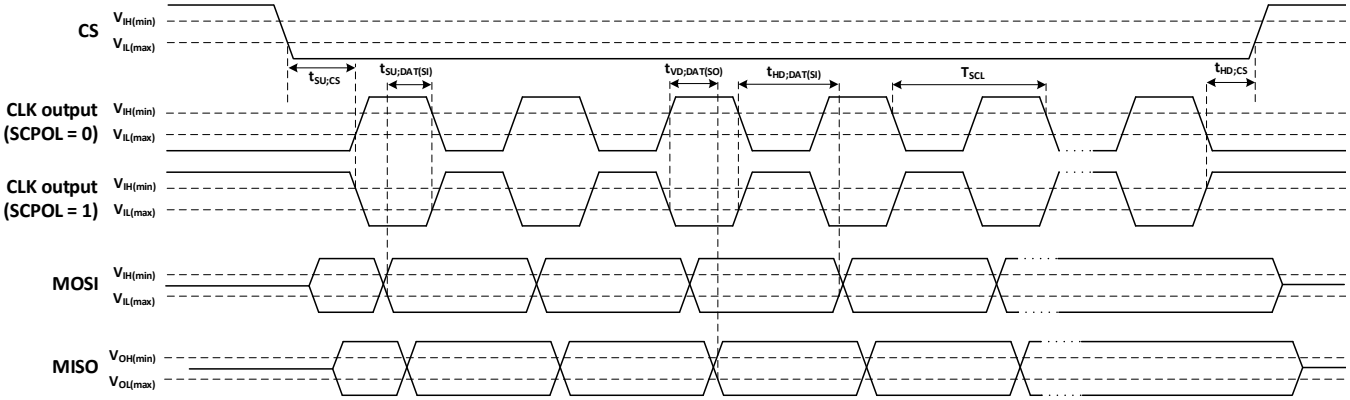


Figure 4-16 Timing diagram for slave (SCPH = 1)

4.16 I2C Characteristics

All measurements are tested under the following conditions:

- The maximum loading is 400pF (SS mode and FS mode), 100pF (HS mode).
- The I/O ports are configured with high driving strength.

Table 4-23 Timing data of I2C (FS/SS mode)

Symbol	Parameter	Standard mode (Cb=400pF max.)		Fast mode (Cb=400pF max.)		Unit
		Min.	Max.	Min.	Max.	
FSCL	SCL clock frequency	-	100	-	400	kHz
$t_{HD;STA}$	Hold time START condition	4	-	0.6	-	µs
t_{LOW}	Low period of the SCL clock	Programmable		Programmable		µs
t_{High}	High period of the SCL clock					µs

t_r	Raise time of both SDA and SCL signals	-	1000	20	300	ns
t_f	Fall time of both SDA and SCL signals	-	300	12	300	ns
$t_{SU;STA}$	Set-up time for a repeated START condition	4.7	-	0.6	-	µs
$t_{HD;DAT}$	Data hold time	0	-	0	-	us
$t_{SU;DAT}$	Data set-up time	0.25	-	0.1	-	µs
$t_{SU;STO}$	Set-up time for STOP condition	4	-	0.6	-	µs
$t_{VD;DAT}$	Data valid time	-	3.45	-	0.9	µs
$t_{VD;ACK}$	Data valid acknowledge time	-	3.45	-	0.9	µs
t_{BUF}	Bus free time between a STOP and START condition	4.7	-	1.3	-	µs

NOTE

Cb is the capacitive load for each bus line.

Table 4-24 Timing data of I2C (HS mode)

Symbol	Parameter	High-Speed mode (Cb=100pF max.)		High-Speed mode (Cb=400pF max.)		Unit
		Min.	Max.	Min.	Max.	
F_{SCL}	SCL clock frequency	-	3.4	-	1.7	MHz
$t_{HD;STA}$	Hold time START condition	160	-	160	-	ns
$t_{SU;STA}$	Set-up time for a repeated START condition	160	-	160	-	ns
$t_{HD;DAT}$	Data hold time	0	70	0	150	ns
$t_{SU;DAT}$	Data set-up time	10	-	10	-	ns
$t_{SU;STO}$	Set-up time for STOP condition	160	-	160	-	ns
t_{high}	High period of the SCL clock	Programmable		Programmable		ns
t_{low}	Low period of the SCL clock					ns
t_{rCL}	Rise time of SCLH signal	-	40	-	80	ns
t_{rCL1}	Rise time of SCLH signal after a repeated START condition and after an acknowledge bit	10	80	20	160	ns
t_{rDA}	Rise time of SDAH signal	10	80	20	160	ns
t_{fCL}	Fall time of SCLH signal	-	40	-	80	ns
t_{fDA}	Fall time of SDAH signal	-	80	-	160	ns

NOTE

Cb is the capacitive load for each bus line.

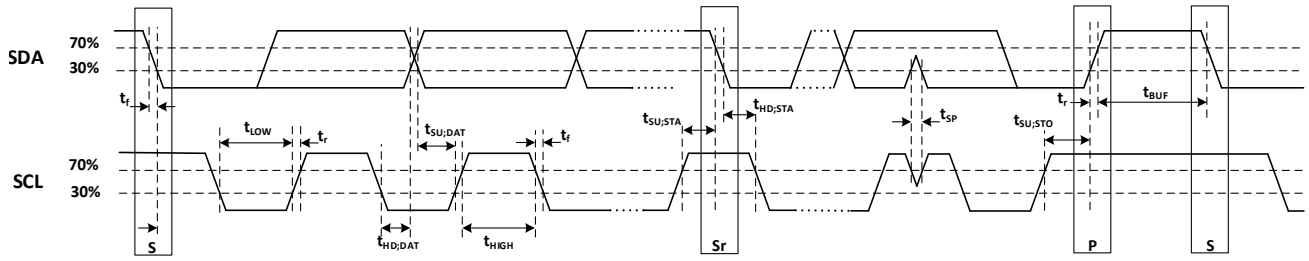


Figure 4-17 Timing diagram of I2C (FS/SS mode)

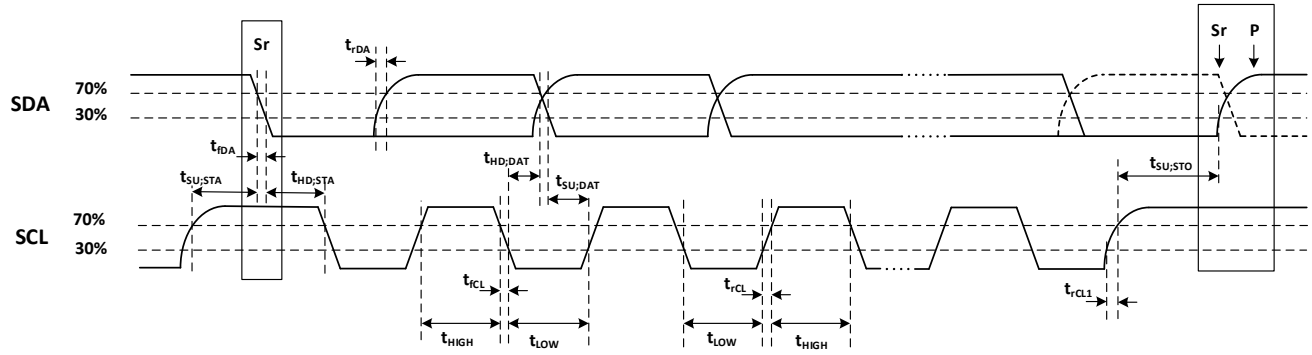


Figure 4-18 Timing diagram of I2C (HS mode)

NOTE

In HS mode, the first rising edge of SCLH signal after a repeated start condition is push-pull output instead of open-drain output.

4.17 I2S Characteristics

The Inter-IC Sound (I2S) supports both master and slave operations.

All measurements are tested under the following conditions:

- The maximum loading is 15pF.
- The I/O ports are configured with high driving strength.

NOTE

Refer to section 4.9 for definitions of $V_{OH(min.)}$, $V_{OL(max.)}$, $V_{IH(min.)}$ and $V_{IL(max.)}$.

Table 4-25 Timing data of I2S

Symbol	Parameter	Conditions	3.3V I/O (2.97V~3.6V)		1.8V I/O (1.71V~1.89V)		Unit
			Min.	Max.	Min.	Max.	
T_{SCL}	I2S clock	Master	82	1953	82	1953	ns
		Slave	82	1953	82	1953	ns
Duty	Clock duty	Master	45	55	45	55	%
		Slave	35	65	35	65	%
$t_{SU;DAT(I)}$	Input data setup time	Master	8	-	8	-	ns
$t_{SU;DAT(I)}$/$t_{SU;WS}$	Input data/WS setup time	Slave	3	-	3	-	ns
$t_{HD;DAT(I)}$	Input data hold time	Master	0	-	0	-	ns
		Slave	3	-	3	-	ns
$t_{VD;DAT(O)}$	Output data valid time	Master	-5	5	-8	8	ns
$t_{VD;WS}$	Output WS valid time	Master	-4	4	-7	7	ns
$t_{VD;DAT(O)}$	Output data valid time	Slave	-	18	-	24	ns

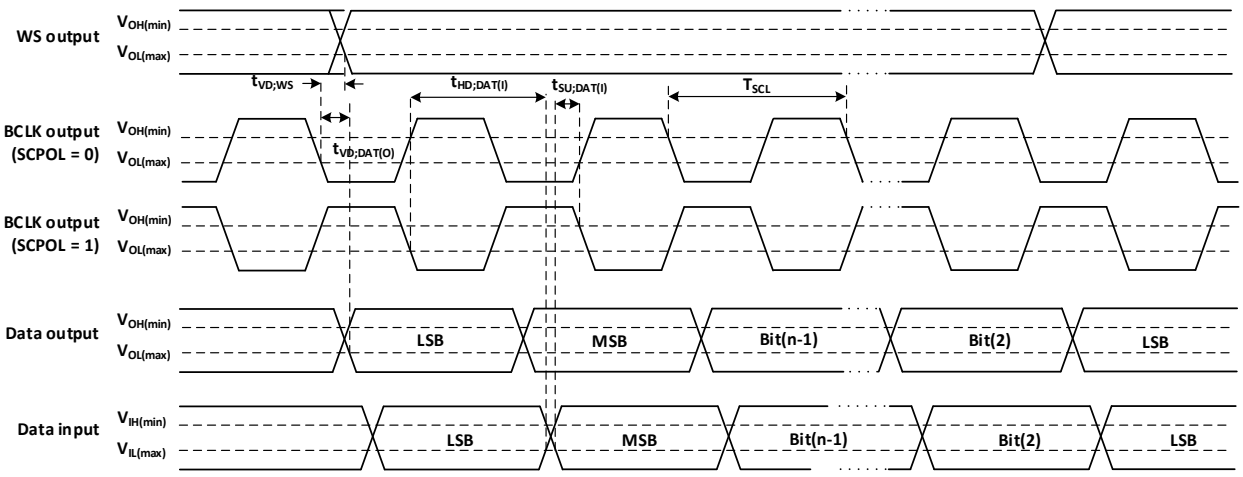


Figure 4-19 Timing diagram for I2S master

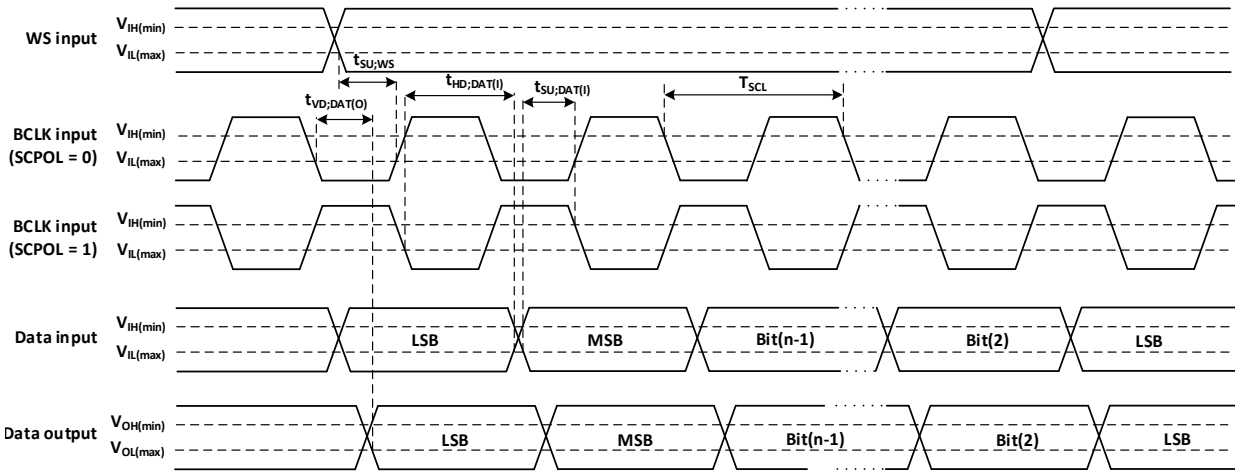


Figure 4-20 Timing diagram for I2S slave

4.18 DMIC Characteristics

The Digital Microphone (DMIC) supports only master operations.

All measurements are tested under the following conditions:

- The maximum loading is 15pF.
- The I/O ports are configured with high driving strength.

NOTE

Refer to section 4.9 for definitions of $V_{OH(min.)}$, $V_{OL(max.)}$, $V_{IH(min.)}$ and $V_{IL(max.)}$.

Table 4-26 Timing data of DMIC

Symbol	Parameter	Condition	3.3V I/O (2.97V~3.6V)		1.8V I/O (1.71V~1.89V)		Unit
			Min	Max	Min	Max	
T_{SCL}	DMIC clock period	Master	200	32000	20	32000	ns
Duty cycle	DMIC clock duty cycle	Master	45	55	45	55	%
$t_{SU;DAT(R)}/t_{SU;DAT(F)}$	Input data rising/falling edge setup time	Master	13	-	13	-	ns
$t_{HD;DAT(R)}/t_{HD;CS(F)}$	Input data rising/falling edge hold time	Master	2	-	2	-	ns

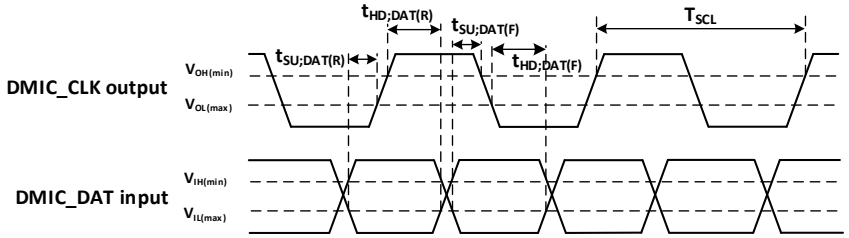


Figure 4-21 Timing diagram of DMIC

4.19 Debug Interface Characteristics

The debug interface of RTL8711Dx is Arm standard bi-directional Serial Wire Debug (SWD).

All measurements are tested under the following conditions:

- The maximum loading is 15pF.
- The I/O ports are configured with high driving strength.

NOTE

Refer to section 4.9 for definitions of $V_{OH(min.)}$, $V_{OL(max.)}$, $V_{IH(min.)}$ and $V_{IL(max.)}$.

Table 4-27 Timing data of SWD

Symbol	Parameter	Conditions	3.3V I/O (2.97V~3.6V)		1.8V I/O (1.71V~1.89V)		Unit
			Min.	Max.	Min.	Max.	
T_{SCL}	SWCLK clock period	Slave	50	-	50	-	ns
Duty cycle	Input clock duty cycle	Slave	30	70	30	70	%
$t_{VD;DAT(O)}$	Output data valid time	Slave	-	14	-	20	ns
$t_{VD;DAT(I)}$	Input data setup time	Slave	2	-	2	-	ns
$t_{HD;DAT(I)}$	Input data hold time	Slave	2	-	2	-	ns

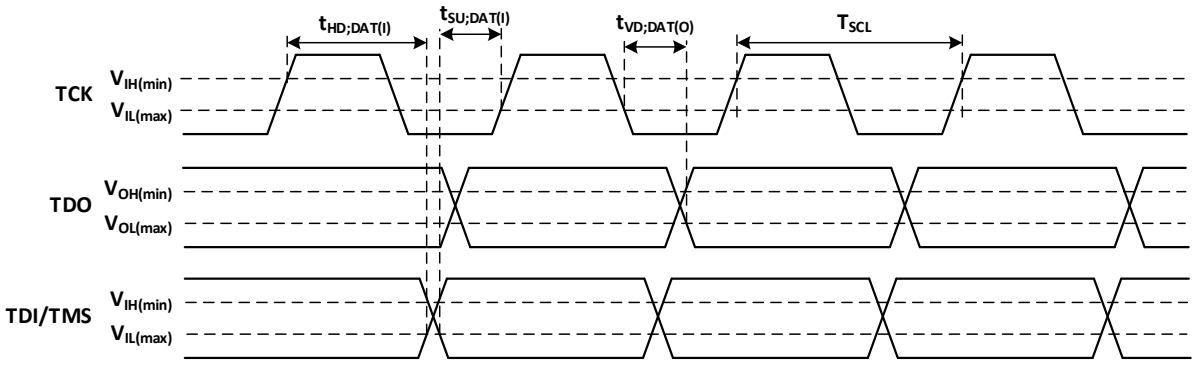


Figure 4-22 Timing diagram of SWD

4.20 LEDC Characteristics

The LEDC is used to control external Intelligent LED lamps by outputting LED data.

Table 4-28 Timing data of LEDC

Symbol	Description	Default value	Value range[1]	Unit
T0H	Digital 0 code, high-level time	300	25 ~ 6375	ns
T0L	Digital 0 code, low-level time	800	25 ~ 6375	ns
T1H	Digital 1 code, high-level time	800	25 ~ 6375	ns
T1L	Digital 1 code, low-level time	300	25 ~ 6375	ns
RESET	Frame unit, low-level time	300	25 ~ 409575	ns
wait_time0[2]	Low-Level time between two pixels' data.	-	25 ~ 12775	ns
wait_time1[2]	Low-Level time after RESET except for the 1th frame	-	25 ~ 5.3e10	ns

NOTE

[1] The adjustment unit of the symbol value is 25ns.
[2] wait_time0 and wait_time1 are optional, default disabled.

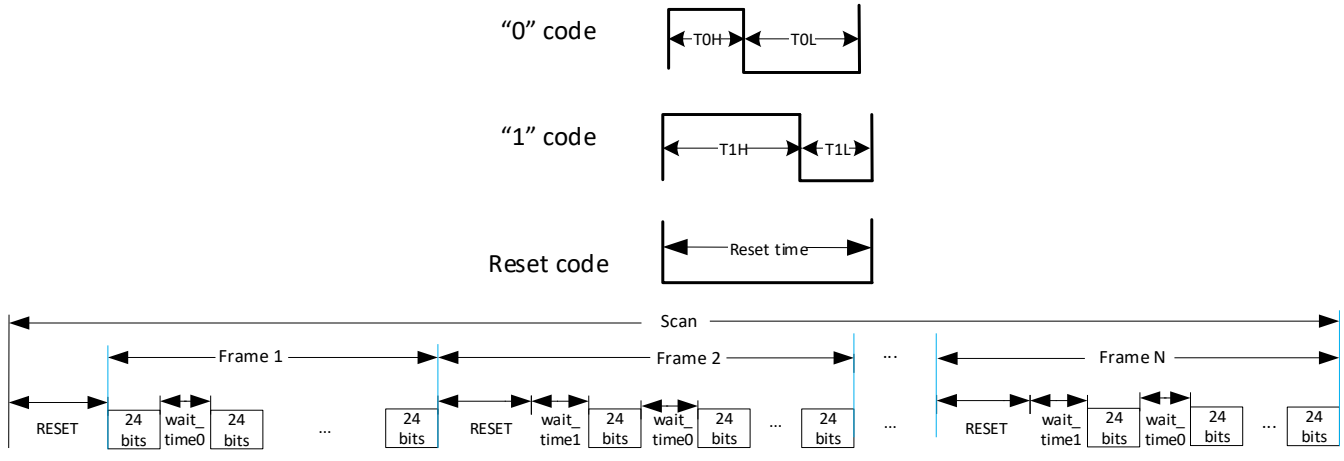


Figure 4-23 LEDC output timing diagram

4.21 OSPI Characteristics

The OSPI of RTL8711Dx has the following features:

- Only supports master operations.
- Limited choices with fixed group usage, that is to say, only the specified pins configured as function ID5 can be used in combination:
  - Group1 (PA12, PA26, PA27, PA30, PA31, PB17~PB21, PA28)
  - Three backup group for Group1
    - PA29, PA26, PA27, PA30, PA31, PB17~PB21, PA28
    - PA12, PB30, PB31, PA30, PA31, PB17~PB21, PA28

- ◆ PA29, PB30, PB31, PA30, PA31, PB17~PB21, PA28
- ■ Group2 (PA19~PA21, PB6~PB9, PB13~PB16)

All measurements are tested under the following conditions:

- The maximum loading is 15pF.
- The I/O ports are configured with high driving strength.

NOTE

Refer to section 4.9 for definitions of $V_{OH(min.)}$, $V_{OL(max.)}$, $V_{IH(min.)}$ and $V_{IL(max.)}$.

Table 4-29 Timing data of OSPI SDR

Symbol	Parameter	Conditions	3.3V I/O (2.97V~3.63V)		1.8V I/O (1.7V~1.95V)		Unit
			Min.	Max.	Min.	Max.	
T_{SCL}	OSPI clock period	Master	20	-	20	-	ns
Duty cycle	OSPI duty cycle		45	55	45	55	%
$t_{su;CS}$	CS setup time		0.5*T_{SCL} -1	-	0.5* T_{SCL} -1	-	ns
$t_{HD;CS}$	CS hold time		T_{SCL} -1	-	T_{SCL} -1	-	ns
$t_{VD;DAT(O)}$	Data output valid time		-4	2	-4	2	ns
$t_{SU;DAT(I)}$	Data input setup time		4	-	4	-	ns
$t_{HD;DAT(I)}$	Data input hold time		2	-	2	-	ns

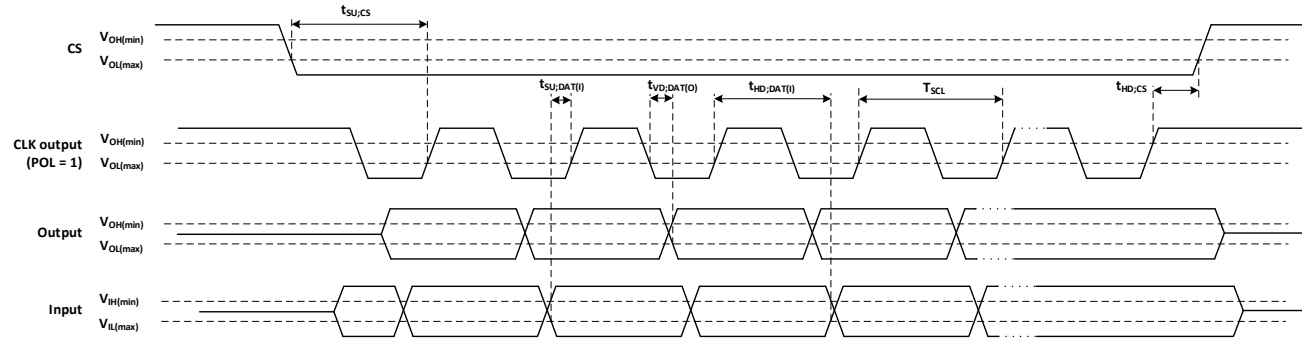


Figure 4-24 Timing diagram of OSPI SDR (PHA=1)

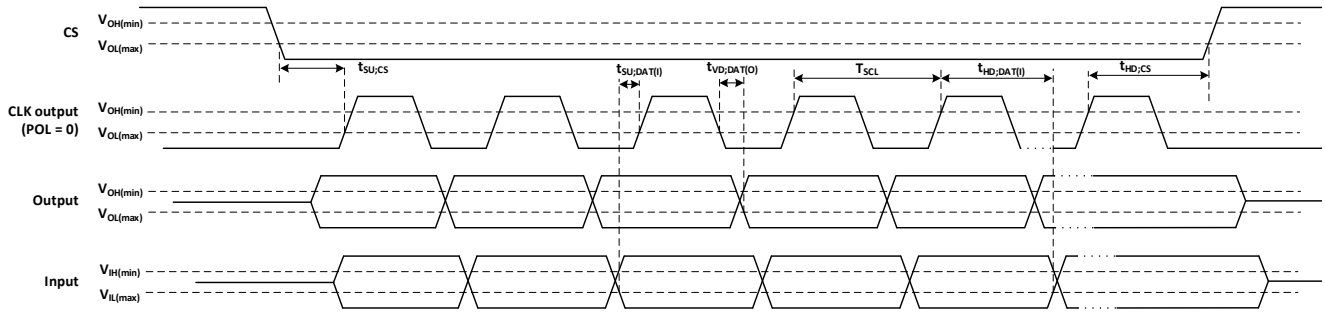


Figure 4-25 Timing diagram of OSPI SDR (PHA=0)

Table 4-30 Timing data of OSPI DDR

Symbol	Parameter	Condition	3.3V I/O (2.97V~3.63V)		1.8V I/O (1.7V~1.95V)		Unit
			Min.	Max.	Min.	Max.	
T_{SCL}	OSPI clock period	Master	20	-	20	-	ns
Duty cycle	OSPI duty cycle		45	55	45	55	%
$t_{su;CS}$	CS setup time		0.5*T_{SCL} -1	-	0.5* T_{SCL} -1	-	ns
$t_{HD;CS}$	CS hold time		T_{SCL} -1	-	T_{SCL} -1	-	ns
$t_{SU;DAT(O)}$	Data input setup time		2	-	2	-	ns
$t_{HD;DAT(O)}$	Data input hold time		6	-	6	-	ns

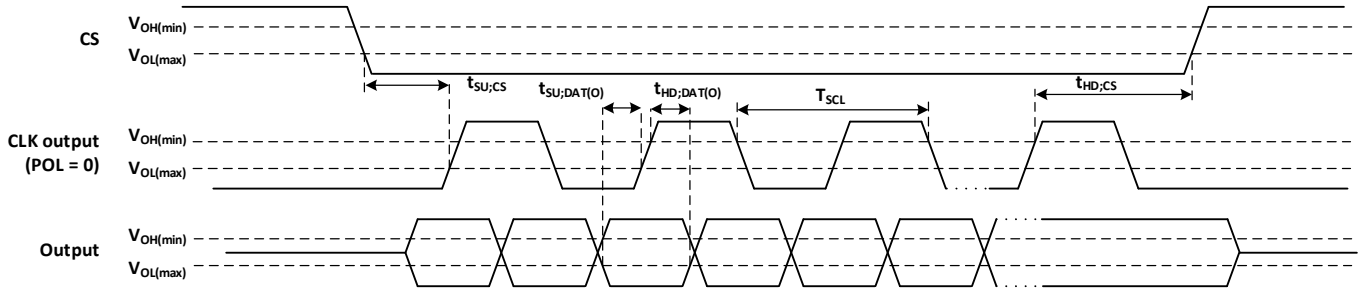


Figure 4-26 Timing diagram of OSPI DDR (PHA=0)

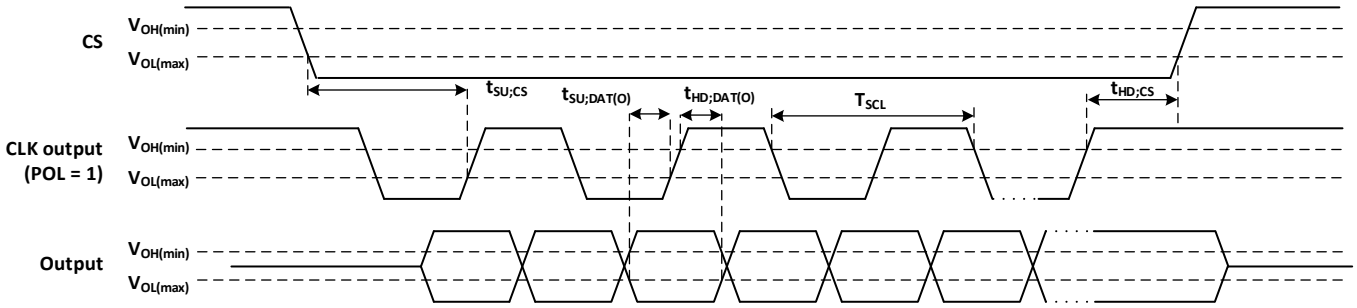


Figure 4-27 Timing diagram of OSPI DDR (PHA=1)

4.22 SDIO Device Characteristics (TBD)

5 Package Information

In order to meet environmental requirements, Realtek offers devices in different grades of ECOPACK® packages, depending on the level of environmental compliance.

5.1 Package Outline

5.1.1 QFN48

The QFN48 is a 48-pin, 6mm x 6mm quad flat no-leads package with 0.4mm pitch.

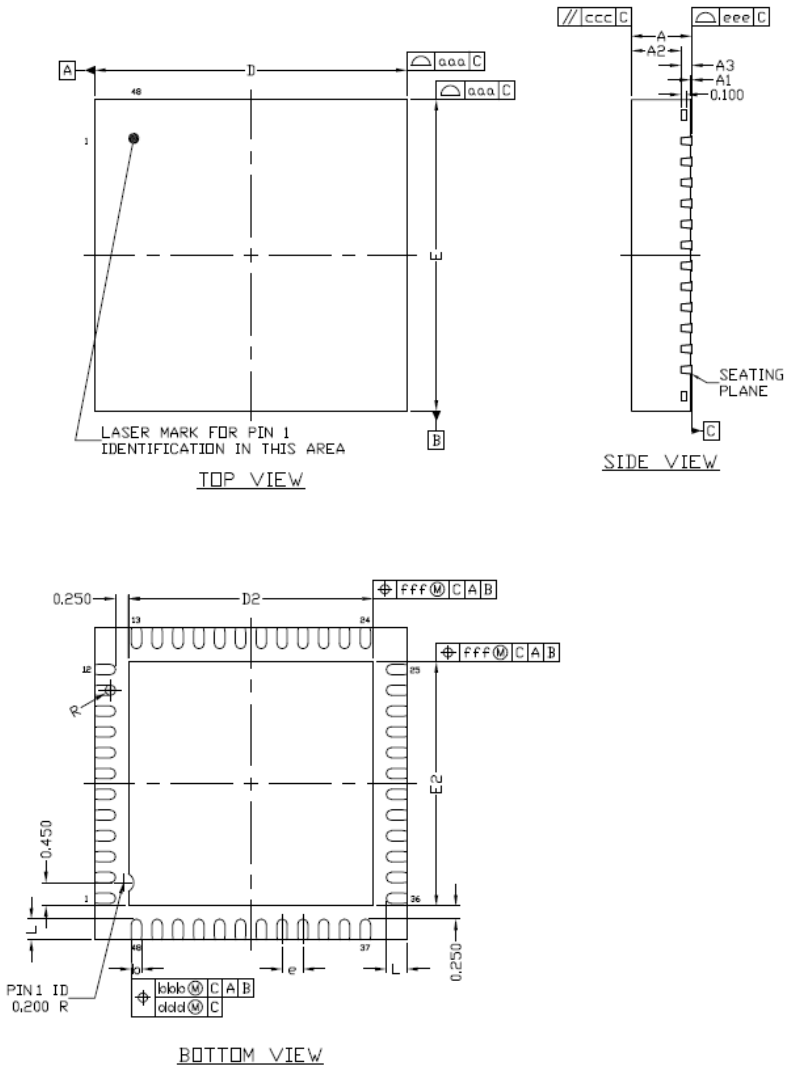


Figure 5-1 QFN48 package outline

Table 5-1 QFN48 package mechanical data

Symbol	Dimension (millimeter)			Dimension (inch)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	1.000	1.100	1.200	0.039	0.043	0.047
A1	0.000	-	0.050	0.000	-	0.002
A2	-	0.950	1.000	-	0.037	0.039
A3	0.203 REF			0.008 REF		
b	0.150	0.200	0.250	0.006	0.008	0.010
D	6.000 BSC			0.236 BSC		

D2	4.600	4.700	4.8000	0.181	0.185	0.189
E	6.000 BSC			0.236 BSC		
E2	4.600	4.70	4.800	0.181	0.185	0.189
L	0.300	0.400	0.500	0.012	0.016	0.020
e	0.400 BSC			0.016 BSC		
R	0.075	-	-	0.003	-	-
TOLERANCES OF FORM AND POSITION						
aaa	0.100			0.004		
bbb	0.070			0.003		
ccc	0.100			0.004		
ddd	0.050			0.002		
eee	0.080			0.003		
fff	0.100			0.004		

NOTE

- *Dimensioning & Tolerances conform to ASME Y14.5M.-1994.*
- *Values in inches are converted from mm and rounded to 3 decimal digits.*

5.1.2 QFN68

The QFN68 is a 68-pin, 8mm x 8mm quad flat no-leads package with 0.4mm pitch.

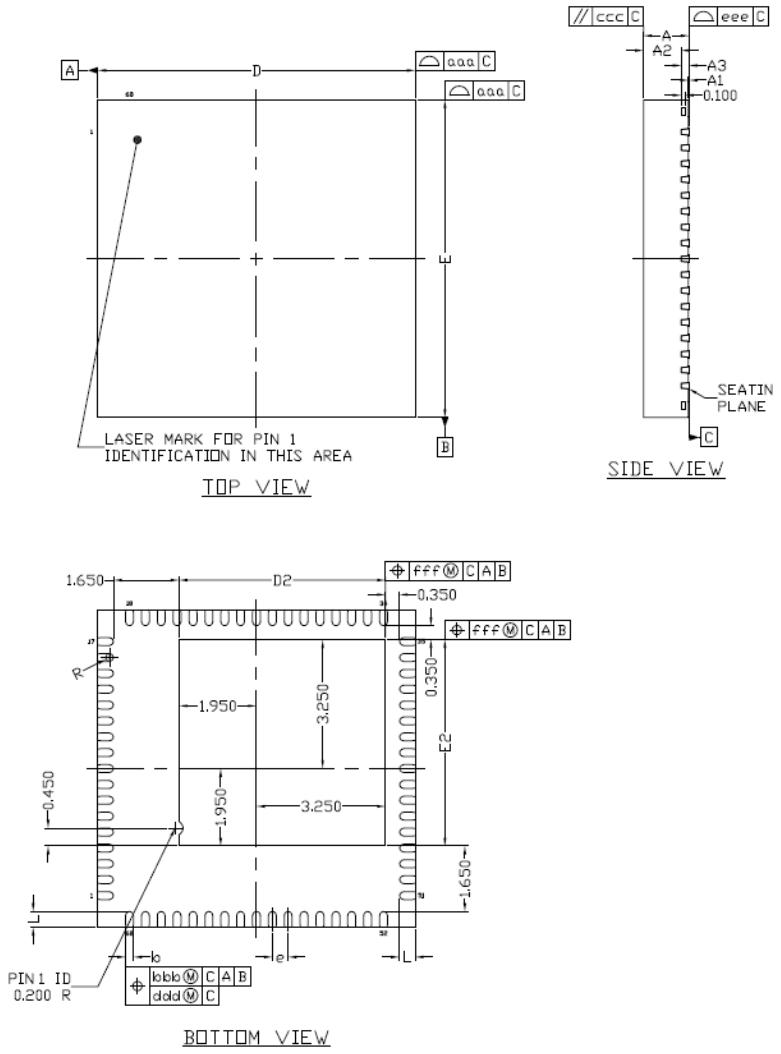


Figure 5-2 QFN68 package outline

Table 5-2 QFN68 package mechanical data

Symbol	Dimension (millimeter)			Dimension (inch)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	1.000	1.100	1.200	0.039	0.043	0.047
A1	0.000	-	0.050	0.000	-	0.002
A2	-	0.950	1.000	-	0.037	0.039
A3	0.203 REF			0.008 REF		
b	0.150	0.200	0.250	0.006	0.008	0.010
D	8.000 BSC			0.315 BSC		
D2	5.100	5.200	5.300	0.201	0.205	0.209
E	8.000 BSC			0.315 BSC		
E2	5.100	5.200	5.300	0.201	0.205	0.209
L	0.300	0.400	0.500	0.012	0.016	0.020
e	0.400 BSC			0.016 BSC		
R	0.075	-	-	0.003	-	-
TOLERANCES OF FORM AND POSITION						
aaa	0.100			0.004		
bbb	0.070			0.003		
ccc	0.100			0.004		
ddd	0.050			0.002		
eee	0.080			0.003		
fff	0.100			0.004		

NOTE

- *Dimensioning & Tolerances conform to ASME Y14.5M.-1994.*
- *Values in inches are converted from mm and rounded to 3 decimal digits.*

5.2 Thermal Characteristics (TBD)

Revision History

Date	Revision	Release Notes
2023-12-19	1.0	Initial release