RTL8720CM-VA2-CG
RTL8720CM-VT2-CG
RTL8720CF-VA2-CG
RTL8720CF-VT2-CG

Ameba ZII
IEEE 802.11b/g/n Compatible
1T1R WLAN + Bluetooth SoC

DATASHEET
(CONFIDENTIAL: Development Partners Only)

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USING THIS DOCUMENT

This document is intended for the software engineer's reference and provides detailed programming information.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

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Do not open the protective conductive packaging until you have read the following, and are at an approved anti-static workstation.

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- Use a conductive wrist strap attached to a good earth ground
- Always discharge yourself by touching a grounded bare metal surface or approved anti-static mat before picking up an ESD-sensitive electronic component
- If working on a prototyping board, use a soldering iron or station that is marked as ESD-safe
- Always disconnect the microcontroller from the prototyping board when it is being worked on

REVISION HISTORY

Revision	Release Date	Summary
1.0	2020/08/31	First release.
1.1	2021/03/03	Added WPA3 support and flash size info. Modified Pin8 (VA11_SYN) to NC. Added section 9.5 ESD Characteristics, page 34.
1.2	2021/05/25	Revised section 3.1 Power Architecture, page 4 (added LDO 3.3V output from 5V). Revised Figure 2 Ameba ZII Regulator Architecture, page 4. Revised Figure 8 Pin Assignments, page 10. Revised Table 4 Power On Trap Pins, page 11 (GPIOA_0). Revised Table 6 Power Pins, page 12 (VDD_IN, VD33_OUT). Added note to Table 10 GPIO Pin Function, page 14. Revised section 7.4 UART Interface, page 21. Added 5V Input/5V UART features. Revised Table 19 Bluetooth Receiver Performance Table-BLE, page 32. Revised Table 22 Power Supply DC Characteristics, page 33. Revised Table 23 Typical Digital IO DC Parameters, page 34. Revised 9.6.1 Power On or Resuming from Deep Sleep Sequence, page 35. Revised Figure 22 Timing Sequence Resume from Standby, page 36. Revised Figure 23 Timing Sequence of Shutdown, page 37. Revised section 11 Ordering Information, page 40. Corrected minor typing errors.

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1. General Description

The Realtek Ameba ZII series are highly integrated single-chips with a low-power IEEE 802.11n Wireless LAN (WLAN) compatible network controller. They combine a Real-M300 (KM4) CPU that is based on ARMv8-M architecture, and integrates a WLAN MAC, an 1T1R capable WLAN baseband, an RF circuit, and Bluetooth Low Energy (BLE) in a single chip. They also provide configurable GPIOs that are configured as digital peripherals for various applications and control usage.

The Ameba ZII series integrates internal memory for full Wi-Fi protocol functions. The embedded memory configuration also enables simple application development.

2. Features

MCU Features

- Real-M300 (KM4) clock frequency up to 100MHz
- I-Cache 32KB/D-Cache 16KB
- Supports DMA
- eXecute In Place (XIP) on flash

Internal Memory

- Supports 384KB ROM
- Supports 256KB RAM
- Supports external flash interface
- Supports MCM embedded 4MB pSRAM (Option, RTL8720CM-Vx2-CG)
- Supports MCM embedded 2MB Flash (Option, RTL8720CF-Vx2-CG)

Wi-Fi Features

- 802.11 b/g/n compatible 1x1, 2.4GHz
- 802.11e QoS Enhancement (WMM)
- Wi-Fi WEP, WPA, WPA2, WPA3, WPS. Open, shared key, and pair-wise key authentication services
- Supports low power Tx/Rx for short-range application
- Supports Antenna diversity
- Frame aggregation for increased MAC efficiency (A-MSDU, A-MPDU)
- Low latency immediate High-Throughput Block Acknowledgement (HT-BA)
- Long NAV for media reservation with CF-End for NAV release
- Integrated balun, PA/LNA

Bluetooth Low Energy

- Bluetooth Low Energy (BLE) 4.2
- Supports LE secure connections
- Supports LE scatternet
- Supports 1 Master/1 Slave

Secure

- Supports secure boot
- Crypto engine: MD5, SHA-1, SHA2-224, SHA2-256, HMAC, AES

Peripheral Interfaces

- 3 x UART interface, baud rate up to 4MHz and all of them can be configurable as log UART
- 1 x I2C, Max clock 400Kbps
- 1 x SDIO 2.0 Device, up to 50MHz
- 1 x SPI, Master clock up to 25Mbps/Slave clock up to 5Mbps
- 8 x PWM with configurable duration and duty cycle from 0 ~ 100%
- 16 x programmable GPIOs (RTL8720CF-Vx2-CG supports 20pins)
- 1 GDMA with 2 channels

Clock Source

- 40MHz crystal oscillator

Package Type

- 5mm x 5mm x 0.85mm
- QFN40 pins

3. Block Diagram

The Ameba ZII diagram shown below provides a general application scenario. External devices can be connected with various peripheral interfaces. The PMU and related blocks for low power application are also shown.

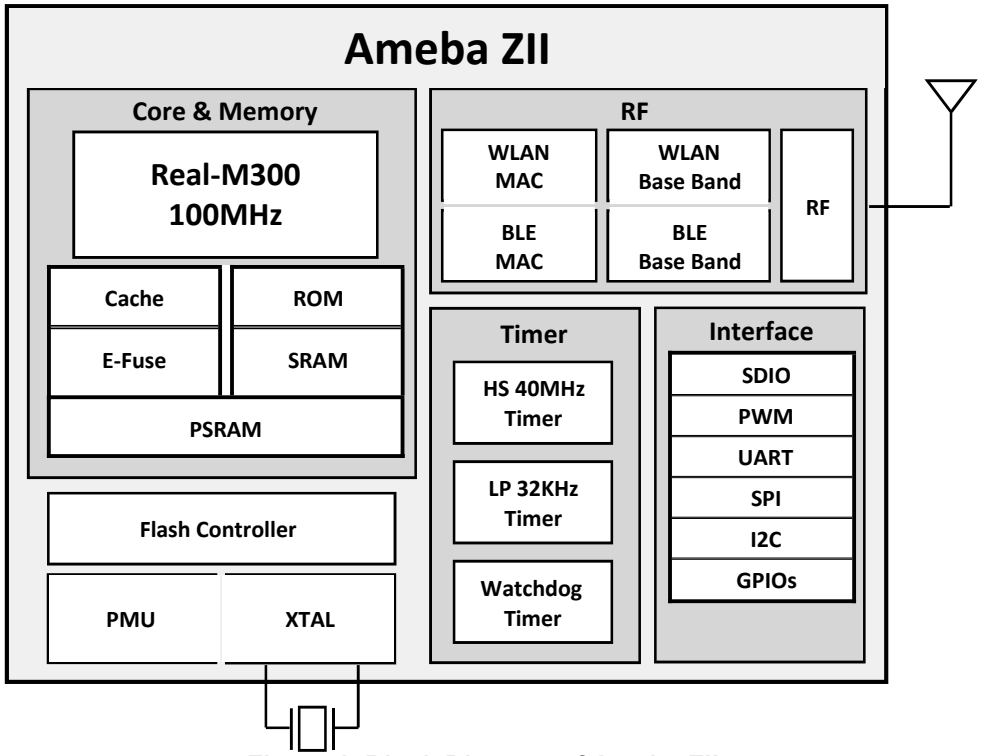


Figure 1. Block Diagram of Ameba ZII

3.1. Power Architecture

Figure 2 shows the Ameba ZII Power Management control Unit architecture.

The PMU provides the following functions:

- SWR 1.1V output from 3.3V (optional for LDO mode)
- LDO 3.3V output from 5V
- LDO 2.5V output for writing E-fuse from 3.3V
- Wakeup system detector to resume from low power state

3.1.1. Ameba ZII Regulator Architecture

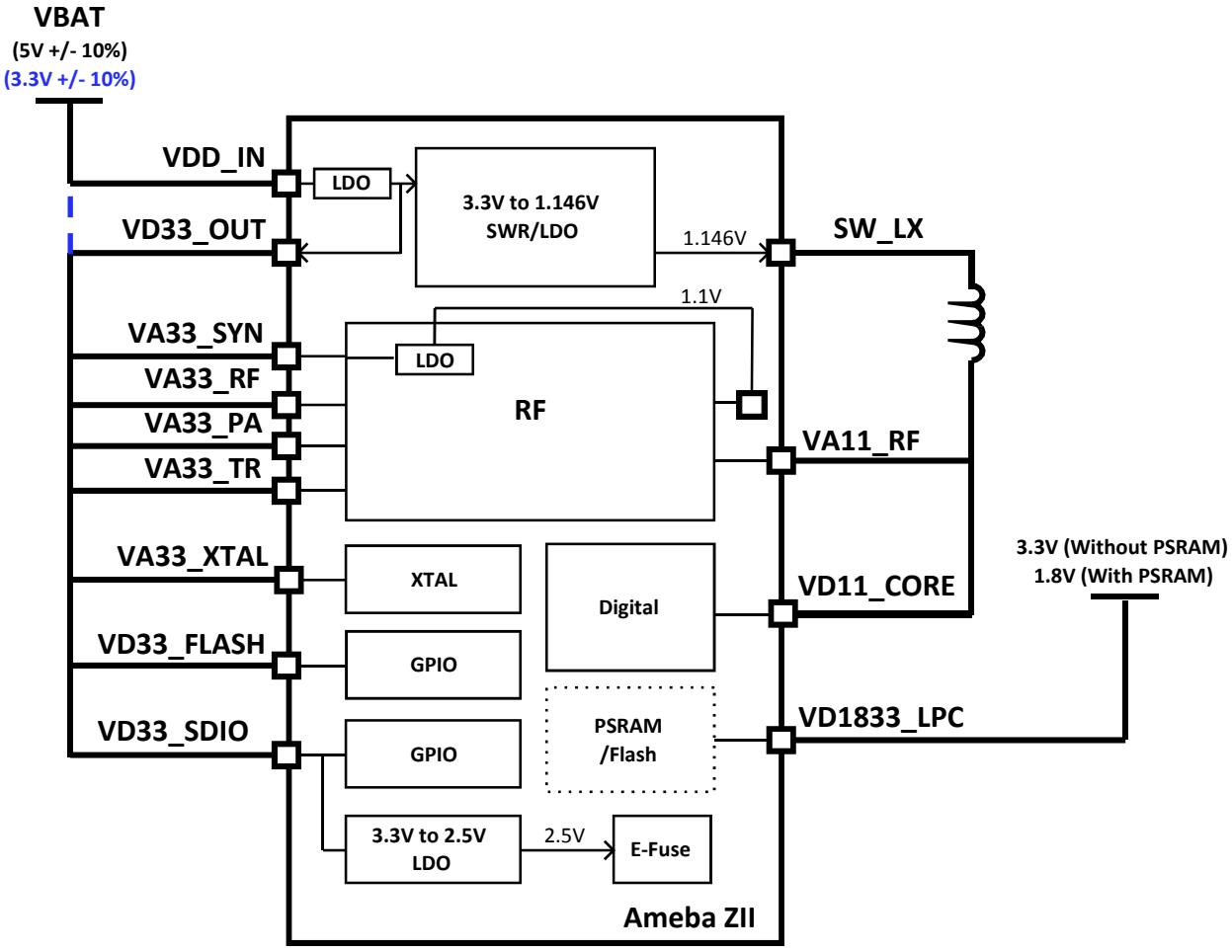


Figure 2. Ameba ZII Regulator Architecture

3.1.2. Shutdown Mode

CHIP_EN de-asserts to shut down the whole chip, without external power cut components required.

CHIP_EN pulled high triggers the system into active mode.

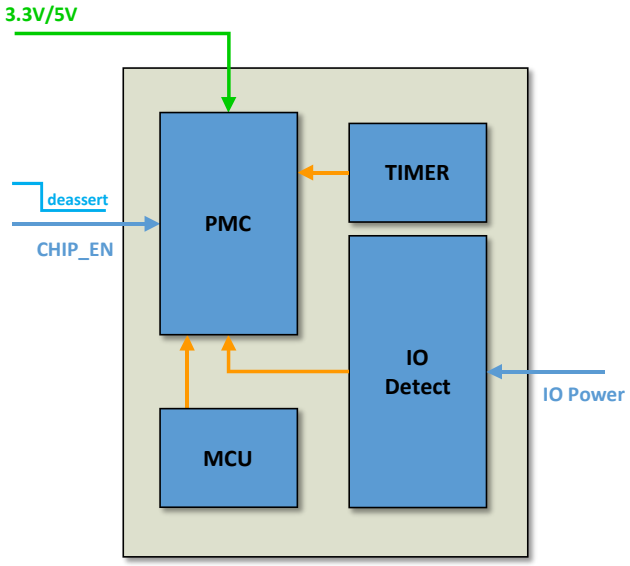


Figure 3. Power Diagram of Shutdown Mode

3.1.3. Deep Sleep Mode

CHIP_EN remains high. Users can invoke the Deep Sleep API to enter deep sleep mode.

Specified interrupts can wake up the system.

The wake flow is:

1. Wake up ISR is high
2. PMC
3. Enable CPU
4. Reboot flow

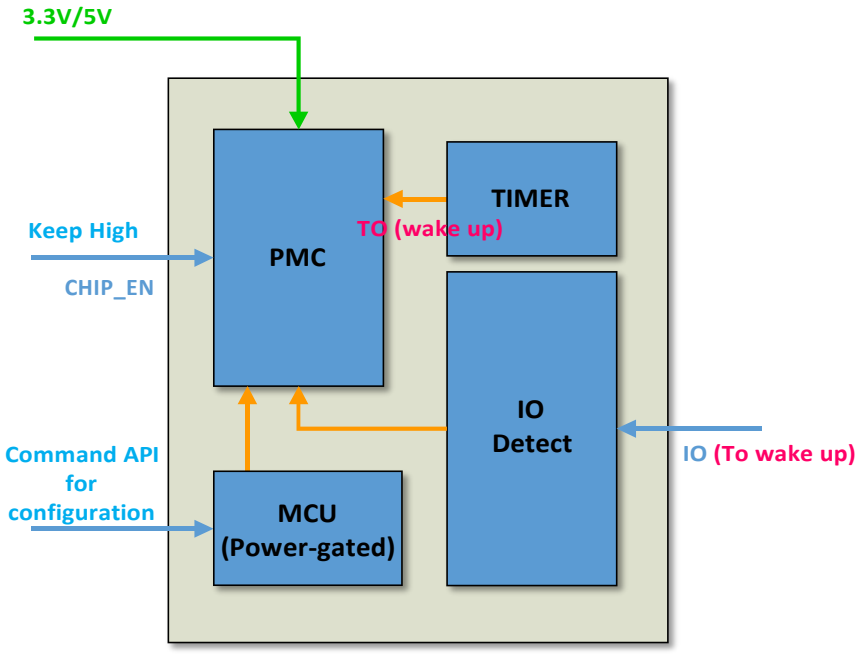


Figure 4. Diagram of Deep Sleep Mode

Table 1. Deep Sleep Mode Wakeup Source

Wakeup Source	Note
Low Precision Timer	-
Wake pin	GPIOA_0, GPIOA_1, GPIOA_2, GPIOA_3, GPIOA_4, GPIOA_7 (depends on package), GPIOA_8 (depends on package), GPIOA_9 (depends on package), GPIOA_10 (depends on package), GPIOA_11 (depends on package), GPIOA_12 (depends on package), GPIOA_13, GPIOA_14, GPIOA_15, GPIOA_16, GPIOA_17, GPIOA_18, GPIOA_19, GPIOA_20, GPIOA_23

3.1.4. Standby Mode

CHIP_EN remains high. Users can invoke the Standby API to enter standby mode.

Specified interrupts can wake up the system.

The wake flow is:

1. Wake up ISR is high
2. PMC
3. Enable CPU
4. Fast reboot flow

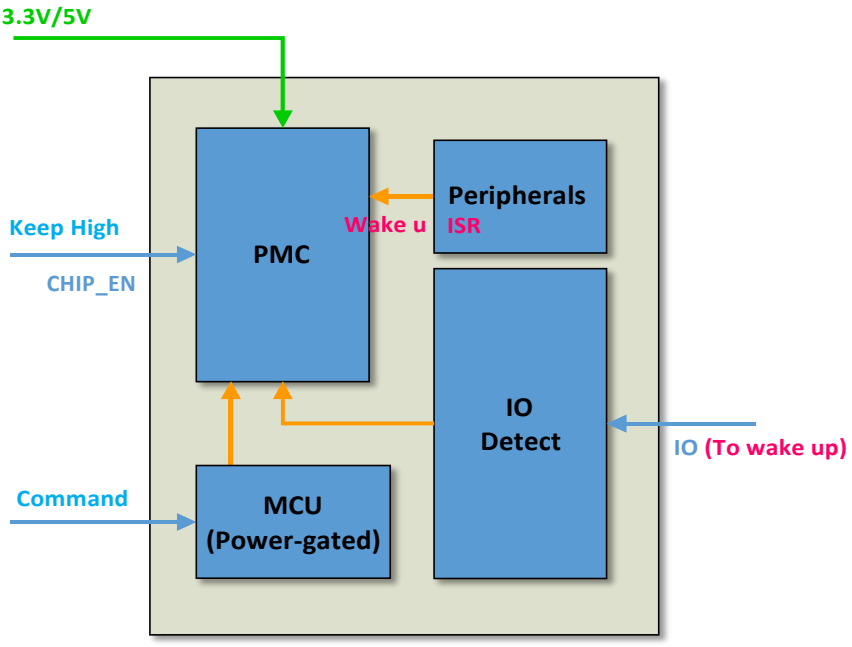


Figure 5. Power Diagram of Standby Mode

Table 2. Standby Mode Wakeup Source

Wakeup Source	Note
Low Precision Timer	-
Wake pin	GPIOA_0, GPIOA_1, GPIOA_2, GPIOA_3, GPIOA_4, GPIOA_7 (depends on package), GPIOA_8 (depends on package), GPIOA_9 (depends on package), GPIOA_10 (depends on package), GPIOA_11 (depends on package), GPIOA_12 (depends on package), GPIOA_13, GPIOA_14, GPIOA_15, GPIOA_16, GPIOA_17, GPIOA_18, GPIOA_19, GPIOA_20, GPIOA_23
UART0	N/A
WLAN	N/A
PWM	N/A
HS Timer	N/A

3.1.5. Sleep Mode

CHIP_EN remains high. Users can invoke Sleep API to enter sleep mode.

Specified interrupts can wake up the system.

The wake flow is:

1. Wake up ISR is high
2. PMC
3. Enable CPU
4. Execution of instructions continues

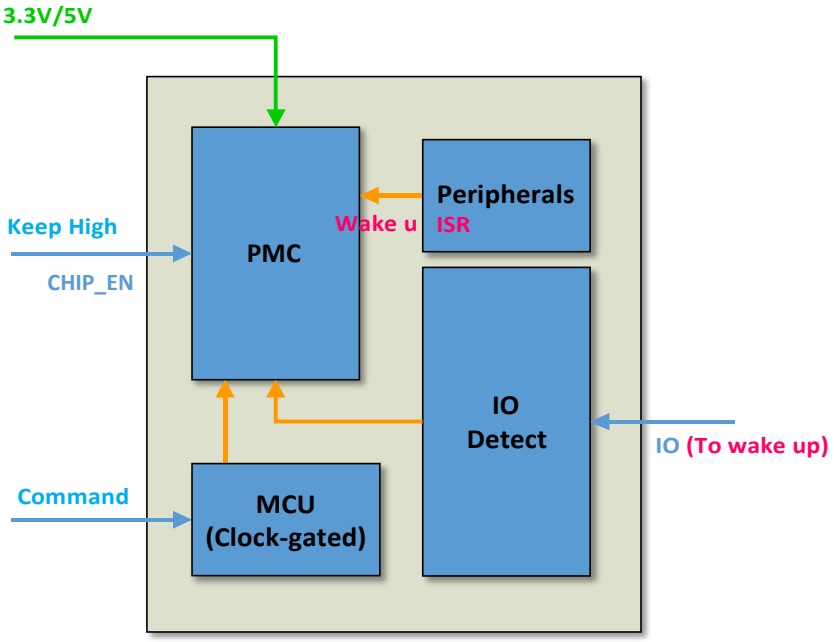


Figure 6. Power Diagram of Sleep Mode

Table 3. Sleep Mode Wakeup Source

Wakeup Source	Note
Low Precision Timer	-
Wake pin	GPIOA_0, GPIOA_1, GPIOA_2, GPIOA_3, GPIOA_4, GPIOA_7 (depends on package), GPIOA_8 (depends on package), GPIOA_9 (depends on package), GPIOA_10 (depends on package), GPIOA_11 (depends on package), GPIOA_12 (depends on package), GPIOA_13, GPIOA_14, GPIOA_15, GPIOA_16, GPIOA_17, GPIOA_18, GPIOA_19, GPIOA_20, GPIOA_23
UART0	N/A
WLAN	N/A
PWM	N/A
HS Timer	N/A
SDIO Device	N/A

3.1.6. Snooze Mode

CHIP_EN remains high. Specified interrupts can wake up the system.

The wake flow is:

1. WLAN power on request
2. Receive particular beacon
3. Wake up ISR is high
4. PMC
5. Enable CPU
6. Execution of instructions continues or fast reboot occurs

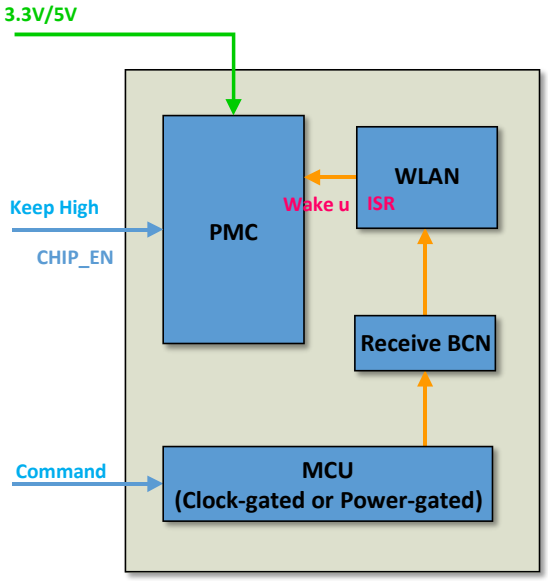


Figure 7. Power Diagram of Snooze Mode

4. Pin Assignments

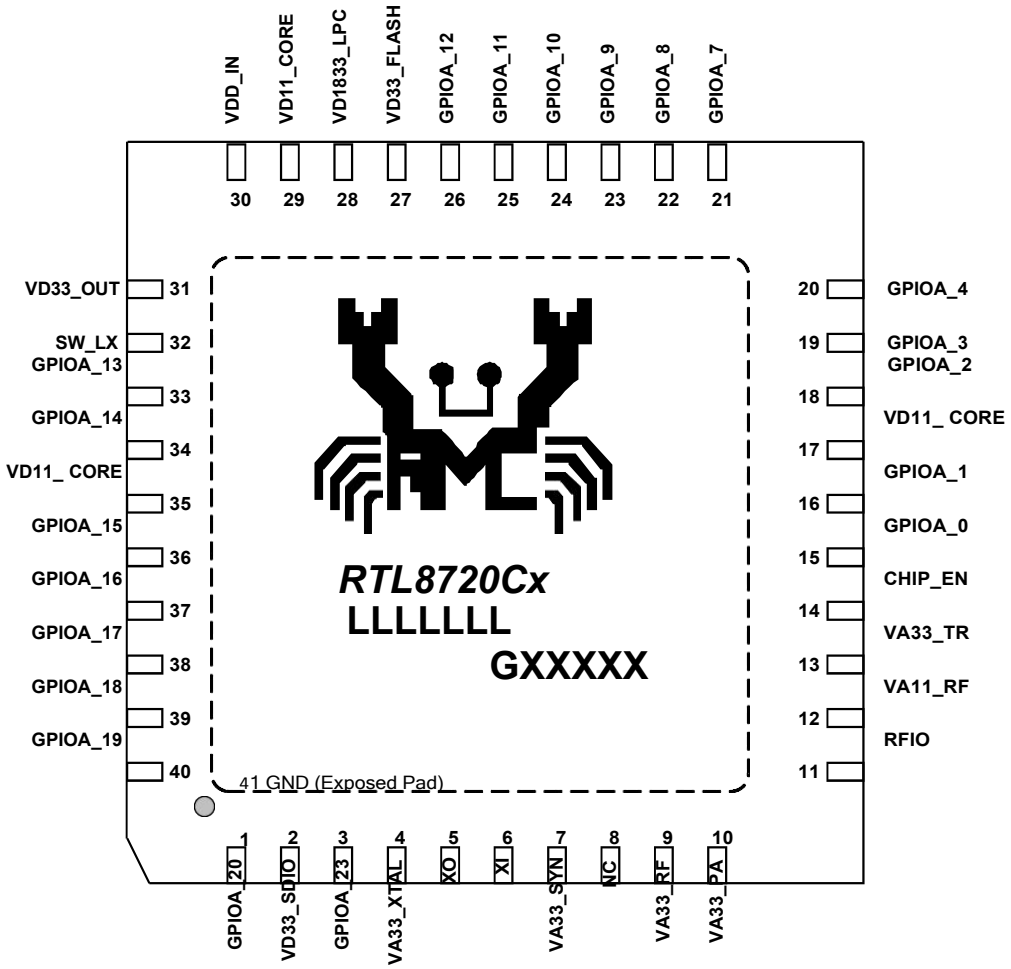


Figure 8. Pin Assignments

4.1. Package Identification

Green package is indicated by the 'G' in GXXXXX in Figure 8.

5. Pin Descriptions

The signal type codes below are used in the following tables:

I: Input O: Output

PI: Power Input PO: Power Output

5.1. Power On Trap Pins

Table 4. Power On Trap Pins

Symbol	Type	Pin No.	Description
GPIOA_0 (TEST_MODE_SEL)	I	15	1: Enter into test/debug mode 0: Normal operation mode (GPIOA_0, GPIOA_13) = (1, 1): Enter into download image mode
GPIOA_1 (Autoload_Fail)	I	16	1: eFUSE settings are not loaded 0: eFUSE settings are loaded
GPIOA_23 (SPS_LDO_SEL)	I	3	1: LDO 0: SWR

5.2. RF Pin

Table 5. RF Pin

Symbol	Type	Pin No.	Description
RF_IO	IO	11	WL RF signal.

5.3. Power Pins

Table 6. Power Pins

Symbol	Type	Pin No.	Description
VD33_SDIO	PI	2	3.3V power for SDIO.
VA33_XTAL	PI	4	3.3V power for XTAL.
VA33_SYN	PI	7	3.3V power for Synthesizer.
VA33_RF	PI	9	3.3V power for RF.
VA33_PA	PI	10	3.3V power for RF PA.
VA11_RF	PI	12	1.15V power for RF.
VA33_TR	PI	13	3.3V power for RF.
VD11_CORE	PI	17	1.15V power for digital core.
VD33_FLASH	PI	27	3.3V power for IO.
VD1833_LPC	PI	28	1.8V power for PSRAM if part number embedded MCM PSRAM. 3.3V power for Flash if part number embedded MCM Flash. 3.3V power for IO if part number without PSRAM/Flash.
VD11_CORE	PI	29	1.15V power for digital core.
VDD_IN	PI	30	5V/3.3V power input.
VD33_OUT	PO PI	31	3.3V output from LDO (when PIN30 VDD_IN is 5V input). 3.3V power (when PIN30 VDD_IN is 3.3V input).
SW_LX	PO	32	1.15V output power from SWR/LDO.
VD11_CORE	PI	35	1.15V power for digital core.

5.4. Clock Pins

Table 7. Clock and Other Pins

Symbol	Type	Pin No.	Description
XI	I	6	Input of 40MHz Crystal Clock Reference.
XO	O	5	Output of 40MHz Crystal Clock Reference.

5.5. Chip EnablePin

Table 8. Chip Enable Pin

Symbol	Type	Pin No.	Description
CHIP_EN	I	14	1: Enable chip 0: Shutdown chip

5.6. Digital IO Pins

Ameba ZII supports a maximum of 20 GPIO pins and all of them are configurable. Refer to Table 9 for detailed information and pin mux rules.

Table 9. GPIO Pins

Symbol	Type	Pin No.	Description
GPIOA_20	IO	1	GPIO pins
GPIOA_23	IO	3	
GPIOA_0	IO	15	
GPIOA_1	IO	16	
GPIOA_2	IO	18	
GPIOA_3	IO	19	
GPIOA_4	IO	20	
GPIOA_7	IO	21	
GPIOA_8	IO	22	
GPIOA_9	IO	23	
GPIOA_10	IO	24	
GPIOA_11	IO	25	
GPIOA_12	IO	26	
GPIOA_13	IO	33	
GPIOA_14	IO	34	
GPIOA_15	IO	36	
GPIOA_16	IO	37	
GPIOA_17	IO	38	
GPIOA_18	IO	39	
GPIOA_19	IO	40	

Note: Default states of all pins are High-impedance; Unused pins should be kept floating.

5.6.1. GPIO Pin Function

Table 10. GPIO Pin Function

Pin Name	SPIC-Flash/SDIO	JTAG	UART	SPI/WL_LED	I2C	PWM
GPIOA_0	-	JTAG_CLK	UART1_IN	-	-	PWM[0]
GPIOA_1	-	JTAG_TMS	UART1_OUT	BT_LED	-	PWM[1]
GPIOA_2	-	JTAG_TDO	UART1_IN	SPI_CSn	I2C_SCL	PWM[2]
GPIOA_3	-	JTAG_TDI	UART1_OUT	SPI_SCL	I2C_SDA	PWM[3]
GPIOA_4	-	JTAG_TRST	UART1_CTS	SPI_MOSI	-	PWM[4]
GPIOA_7	SPI_M_CS	-	-	SPI_CSn	-	-
GPIOA_8	SPI_M_CLK	-	-	SPI_SCL	-	-
GPIOA_9	SPI_M_DATA[2]	-	UART0_RTS	SPI_MOSI	-	-
GPIOA_10	SPI_M_DATA[1]	-	UART0_CTS	SPI_MISO	-	-
GPIOA_11	SPI_M_DATA[0]	-	UART0_OUT	-	I2C_SCL	PWM[0]
GPIOA_12	SPI_M_DATA[3]	-	UART0_IN	-	I2C_SDA	PWM[1]
GPIOA_13	-	-	UART0_IN	-	-	PWM[7]
GPIOA_14	SDIO_INT	-	UART0_OUT	-	-	PWM[2]
GPIOA_15	SD_D[2]	-	UART2_IN	SPI_CSn	I2C_SCL	PWM[3]
GPIOA_16	SD_D[3]	-	UART2_OUT	SPI_SCL	I2C_SDA	PWM[4]
GPIOA_17	SD_CMD	-	-	-	-	PWM[5]
GPIOA_18	SD_CLK	-	-	-	-	PWM[6]
GPIOA_19	SD_D[0]	-	UART2_CTS	SPI_MOSI	I2C_SCL	PWM[7]
GPIOA_20	SD_D[1]	-	UART2_RTS	SPI_MISO	I2C_SDA	PWM[0]
GPIOA_23	-	-	-	LED_0	-	PWM[7]

Note: GPIOA_13/GPIOA_14 can operate in 3.3V or 5V in case selected as UART function when VDD_IN is 5V input; other UART pins operate in 3.3V only.

6. Memory Organization

6.1. Memory Architecture

Ameba ZII integrates ROM, internal SRAM, and extended NOR flash to provide applications with a variety of memory requirements.

6.1.1. Internal ROM

The internal integration of 384KB ROM provides high access speed and low memory leak. The ROM memory clock speed is up to 100MHz.

The ROM lib provides the following functions:

- Boot Code and MCU initialization
- Peripheral Drivers & API
- Non-flash booting functions and drivers
- Security function libs

6.1.2. Internal SRAM

The maximum internal integration of 256KB SRAM provides instruction, data, and buffer usage. The maximum clock speed is up to 100MHz.

6.2. Memory Mapping

The Memory map includes all available memory and register offsets in Ameba ZII.

6.2.1. Programming Space

Table 11. Programming Space Design for Software Instruction Storage

Start Address	Size	Secure	Cache Support	IP Function
0x0000_0000	384KB	Configurable	-	ITCM ROM
0x1000_0000	256KB	Configurable	-	TCM SRAM
0x2000_0000	32KB	Non-Secure	V	Additional SRAM for BT

6.2.2. IO Space

The address map of each peripheral hardware is shown below.

Table 12. Address Map of Each Peripheral Hardware

Start Address	Size	Secure	Cache Support	IP Function
0x2000_0000	32KB	Non-secure	V	Additional SRAM for BT
0x4000_0000	2KB	Non-secure	-	SYS Control (SYSON)
0x4000_1000	2KB	Non-secure	-	GPIO
0x4000_1C00	1KB	Non-secure	-	PWM
0x4000_2000	4KB	Non-secure	-	HS Timer
0x4000_3000	1KB	Non-secure	-	UART0
0x4000_3800	2KB	Non-secure	-	LP Timer
0x4002_0000	4KB	Non-secure	-	SPI Flash Controller
0x4004_0000	1KB	Non-secure	-	UART1
0x4004_0400	1KB	Non-secure	-	UART2
0x4004_2000	1KB	Non-secure	-	SPI
0x4004_4000	1KB	Non-secure	-	I2C
0x4005_0000	16KB	Non-secure	-	SDIO Device
0x4006_0000	2KB	Non-secure	-	GDMA
0x4007_0000	16KB	Non-secure	-	Crypto Engine
0x4008_0000	256KB	Non-secure	-	WLAN
0x4060_0000	4KB	Non-secure	-	pSRAM Controller
0x5000_0800	2KB	Secure	-	SYS Control (SYSON)
0x5000_2000	4KB	Secure	-	HS Timer
0x5006_0000	2KB	Secure	-	GDMA
0x5007_0000	16KB	Secure	-	Crypto Engine

6.2.3. Extension Memory Space

The external flash memory address base is from 0x9800_0000 to 0x9BFF_FFFF.

Table 13. Address Map of Extension Memory Hardware

Name	Physical Address	Size	IP Function
Flash	0x9800_0000	64MB	External flash memory
	0x9BFF_FFFF		

6.3. SPI NOR Flash

Ameba ZII supports NOR flash via SPI interface.

SPI NOR Flash Features:

- SPI baud rate supports 50/33/25/20MHz
- Supports eXecute In Place (XIP)
- Supports memory-mapped I/O interface for read operation
- Supports 32K/16K I/D read cache, 4-way associative
- Supports decryption on the fly
- Supports SPI mode (SPI/Dual SPI/DIO SPI/Quad SPI/QIO SPI)
- Supported flash size: Up to 64 MB

7. Peripheral Interface Descriptions

7.1. General Purpose DMA Controller

The Realtek Direct Memory Access Controller (RTK-DMAC) is a DMA controller with AXI interface. Usually, the CPU sends sequential read/write commands controlling data transfer. However, the CPU cannot execute instructions when it is handling the transfer. To release CPU resources, the DMAC can manage the data transfer completely. The CPU configures DMAC registers to setup a transfer and then enables the channel to start the transfer. The CPU does not have to handle the transfer until there is a DMAC trigger interrupt. The DMAC interrupt is generated when the transfer is done, or the transfer encounters errors.

GDMA Features

- Advanced eXtensible Interface 4 (AXI4) master interface and Advanced Peripheral Bus 3(APB3) slave interface
- 32 bits data bus width
- Two channels. Each channel can be configured with an independent source address and destination address to initiate a transfer. The channel has a proprietary FIFO to push or pop data
- The maximum transfer length per transfer is up to 4095 data items. Each data item can be configured to 1 byte, 2 bytes, or 4 bytes width
- DMA hardware request interface
  - Handshake interface with peripherals to control data flow
- Transfer abort feature
  - The transfer can be stopped safely. The DMAC reports the correct data length already received or transmitted after the termination
- Secure mode access
  - Secure access control for master interface. Non-authorized access cannot access data

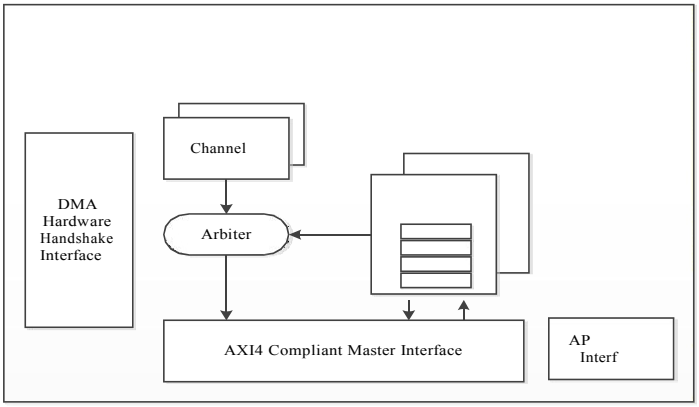


Figure 9. RTL8710C RTK-DMAC Block Diagram

7.2. General Purpose Timer (GTimer)

For various system timing or flow control usage, the general purpose timer provides a counter and timer mode that can be used for any type of time related event generation or timing measurement.

GTIMER Features

- 8 GTimers supported at HS domain; the source clock is from 40MHz
- 1 GTimer supported at LP domain; the source clock is from 32kHz
- Supports counter mode and timer mode
- Each GTimer supports 4 match events

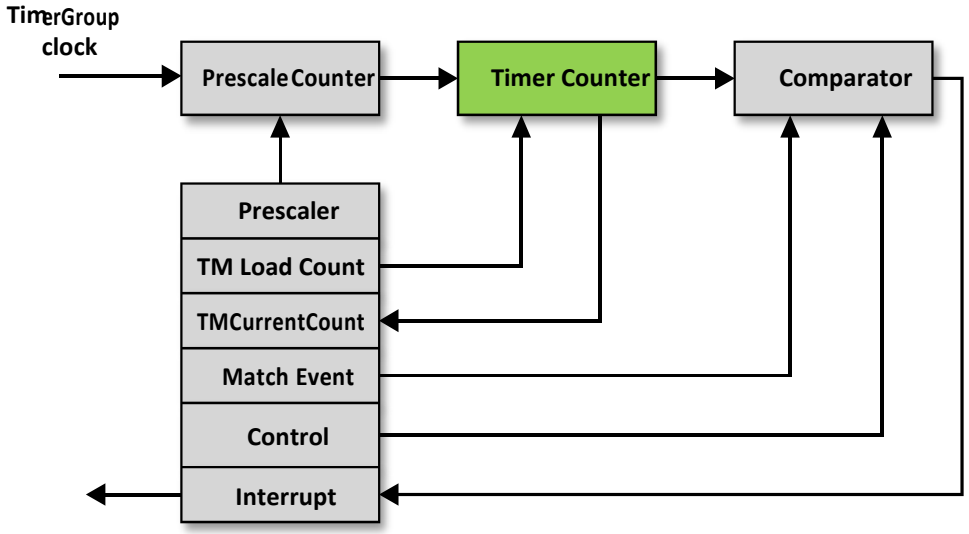


Figure 10. GTimer Functional Diagram

7.3. GPIO Functions

Each of the General Purpose Input/Output (GPIO) pins are software configurable as an output or as an input. In embedded system design, integration and control between different devices and the SoC chip are significant when planning a new architecture system. For the SoC chip, the most essential approach for interfacing external devices of the SOC chip is via the GPIO interfaces. This can provide simple digital input/output IO control. A simple IO pad architecture is shown in Figure 11.

GPIO Features

- GPO and GPI functions
- Supports interrupt detection with configurable polarity per GPIO
- Internal weak pull up and pull low per GPIO
- Multiplexed with other specific digital functions

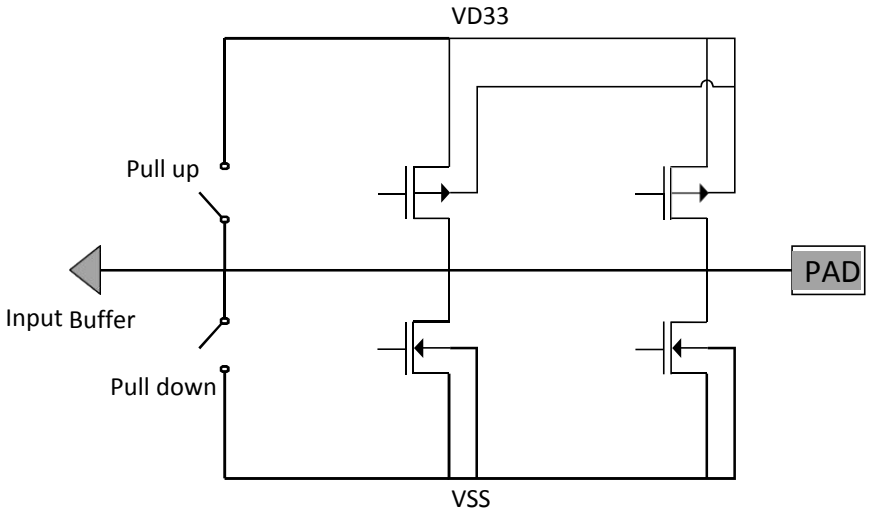


Figure 11. IO Pad Architecture

7.4. UART Interface

UART is a popular serial interface for system information, debug logs and device information exchange. UART supports hardware acceleration such as transmit/receive data FIFO, DMA transfer etc., which makes UART easier to use.

The UART signal level is 3.3V or 5V[1]. The host provides the power source with the targeted power level to the UART interface via the IO power.

UART Features

- Supports 3xUART (max baud rate 4MHz and DMA mode)
- UART (RS232 Standard) Serial Data Format
- Programmable Asynchronous Clock Support
- 16 bytes Transmit Data FIFO and 32 bytes Receive Data FIFO
- Programmable Receive Data FIFO Trigger Level
- Auto Flow Control
- DMA data moving support to reduce CPU loading

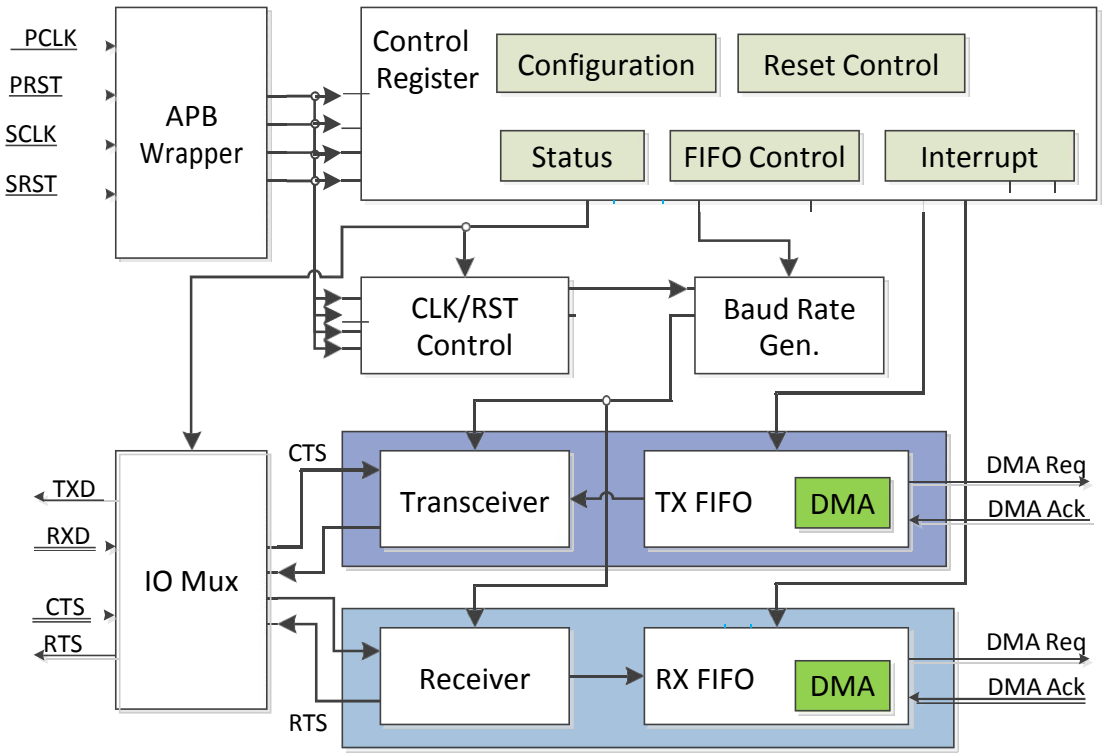


Figure 12. UART Functional Diagram

Note: Only the specified pins can operate in 5V. See section 5.6.1 for details.

7.4.1. UART Specification

The UART interface is a standard 4-wire interface with RX, TX, CTS, and RTS. The default baud rate is 115.2k bit/s. Table 14 shows baud-rate error calculations.

Table 14. UART Baud Rate Specifications

Desired Baud Rate	Actual Baud Rate	Error (%)	Desired Baud Rate	Actual Baud Rate	Error (%)
110	110.0533759	0.048523534	380400	380952.381	0.145210555
300	300.120048	0.040016006	460800	460732.9843	0.014543339
600	600.240096	0.040016006	500000	500000	0
1200	1200.480192	0.040016006	921600	922431.8658	0.090263219
2400	2400.960384	0.040016006	1000000	1000000	0
4800	4801.920768	0.040016006	1382400	1383647.799	0.090263219
9600	9603.841537	0.040016006	1444400	1452145.215	0.536223658
14400	14414.41441	0.1001001	1500000	1506849.315	0.456621005
19200	19230.76923	0.16025641	1843200	1856540.084	0.723745898
28800	28860.02886	0.208433542	2000000	2000000	0
38400	38461.53846	0.16025641	2100000	2105263.158	0.250626566
57600	57720.05772	0.208433542	2764800	2784810.127	0.723745898
76800	76923.07692	0.16025641	3000000	3013698.63	0.456621005
115200	115243.583	0.037832489	3250000	3283582.09	1.033295063
128000	128205.1282	0.16025641	3692300	3728813.559	0.988910959
153600	153846.1538	0.16025641	3750000	3793103.448	1.149425287
230400	231092.437	0.300536881	4000000	4000000	0

7.5. SDIO Device Mode Interface

The SDIO (Secure Digital Input Output) is an extension of the SD specification to cover I/O functions.

SDIO Features

- Supports SDIO 2.0 High Speed mode
- CIS can be configured with internal non-volatile memory for fast card detection
- Realtek SPI provides high efficiency SPI interface with interrupt and full duplex mode
- Supports high performance Ethernet to Wi-Fi transformation
- Supports non-flash booting when using an Ethernet to Wi-Fi transformation card

7.5.1. Bus Timing Specification

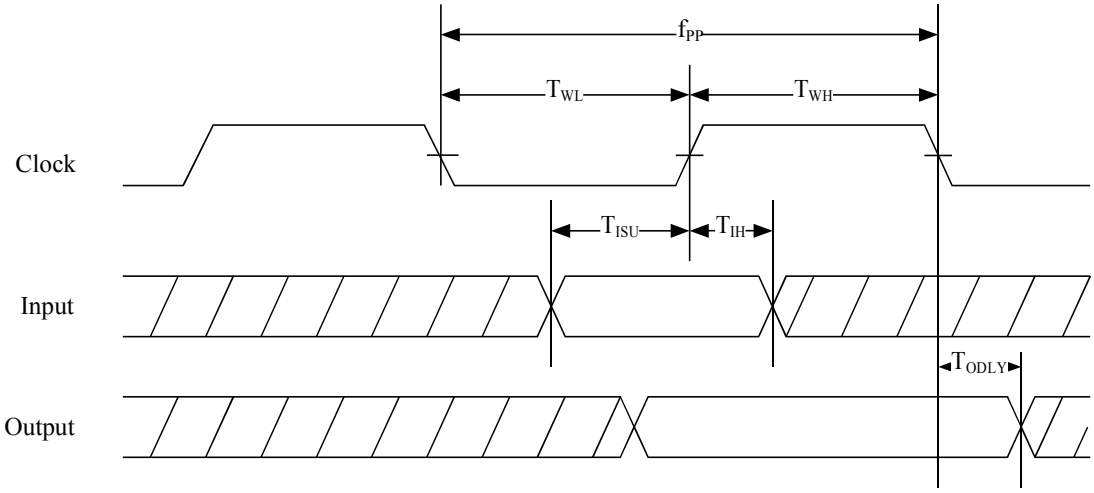


Figure 13. SDIO Interface Timing Sequence

Table 15. SDIO Interface Timing Parameters

Name	Parameter	Mode	Min	Max	Unit
f_{PP}	Clock Frequency	Default	0	25	MHz
		HS	0	50	MHz
T_{WL}	Clock Low Time	Default	10	-	ns
		HS	7	-	ns
T_{WH}	Clock High Time	Default	10	-	ns
		HS	7	-	ns
T_{ISU}	Input Setup Time	Default	5	-	ns
		HS	6	-	ns
T_{IH}	Input Hold Time	Default	5	-	ns
		HS	2	-	ns
T_{ODLY}	Output Delay Time	Default	-	14	ns
		HS	-	14	ns

7.6. SPI Interface

The Serial Peripheral Interface (SPI) enables data communication between microcontrollers and other peripherals. High throughput and full-duplex capability with a simple hardware interface makes the SPI very efficient for various applications. The SPI is widely adopted to communicate with a variety of peripherals including sensors, control devices, memory, LCD, SD cards etc.

SPI Features

- Supports 1 SPI port
- Supports Master/Slave mode
- Multiple Serial Interface Operations supported:
  - Motorola – SPI
  - Texas Instruments – SSI
  - National Semiconductor – Microwire
- Supports DMA to offload CPU bandwidth
- Maximum speed support for each SPI interface:
  - Supports baud rate up to 25MHz (Master mode)
  - Supports baud rate up to 6.25MHz (Slave mode Rx only)
  - Supports baud rate up to 5MHz (Slave mode TRx)
- Programmable clock bit-rate
- Programmable clock polarity (SCPOL) and phase (SCPH) for SPI protocol
- Supports 8 bit and 16 bit data frame size
- Supports bit swapping and byte swapping features
- The transmit FIFO and receive FIFO depth is 1024 bit (up to 64 data frames)

7.6.1. SPI Protocol

The SPI protocol mode can control via 2 parameters, SCPOL and SCPH. Both SCPOL and SCPH can be configured as 0 or 1 (SCPOL = 0/1, SCPH = 0/1) with a total of 4 modes as shown below.

- SCPOL defines inactive state of serial clock status:
  - 0: Low
  - 1: High
- SCPH defines serial clock toggle timing of the first data bit:
  - 0: Middle of the first data
  - 1: Start of the first data

SCPOL=0/SCPH=0:

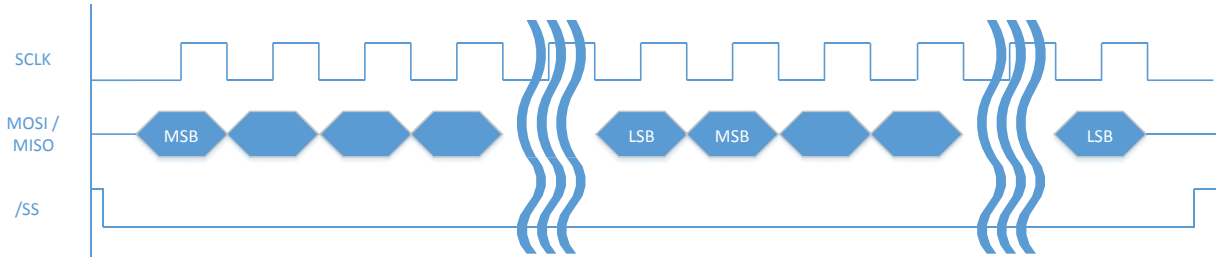


Figure 14. SPI Protocol: Mode 0 (SCPOL=0/SCPH=0)

SCPOL=0/SCPH=1:

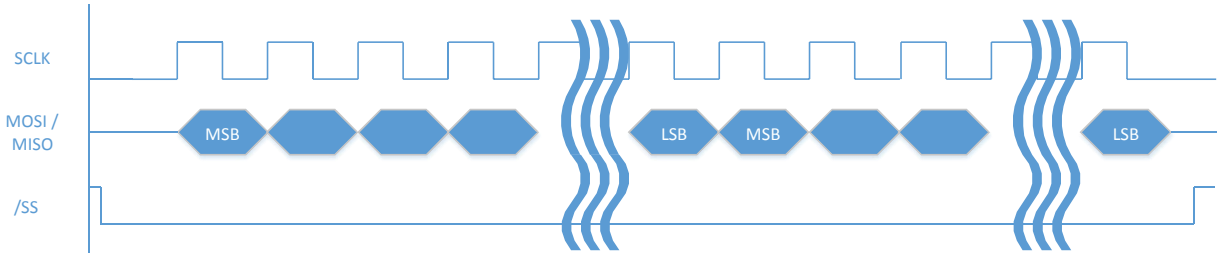


Figure 15. SPI Mode Protocol: Mode 1 (SCPOL=0/SCPH=1)

SCPOL=1/SCPH=0:

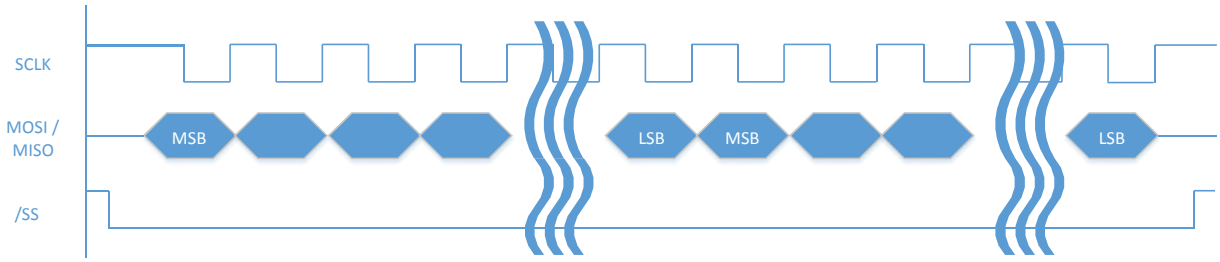


Figure 16. SPI Mode Protocol: Mode 2 (SCPOL=1/SCPH=0)

SCPOL=1/SCPH=1:

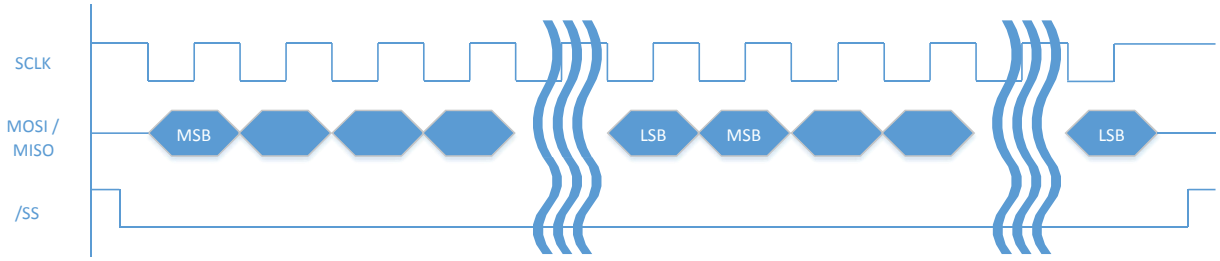


Figure 17. SPI Mode Protocol: Mode 3 (SCPOL=1/SCPH=1)

7.7. I2C Interface

For external device connection, I2C is another popular serial interface since all I2C devices can be connected together, and only two wires (data and clock pin) are required for the I2C protocol. In a pin-limited system, I2C would be the ideal interface to integrate different external elements.

I2C Features

- Supports maximum 1 x I2C ports
- Supports 3 different speeds:
  - Standard mode (0 to 100 Kb/s)
  - Fast mode (<400 Kb/s)
  - High-speed mode (<3.4 Mb/s) (with appropriate bus loading)
- Master or slave I2C operations
- 7-bit/10-bit addressing
- Supports Interrupt or polled mode operation
- Supports TX and RX DMA
- Transmit and receive buffers

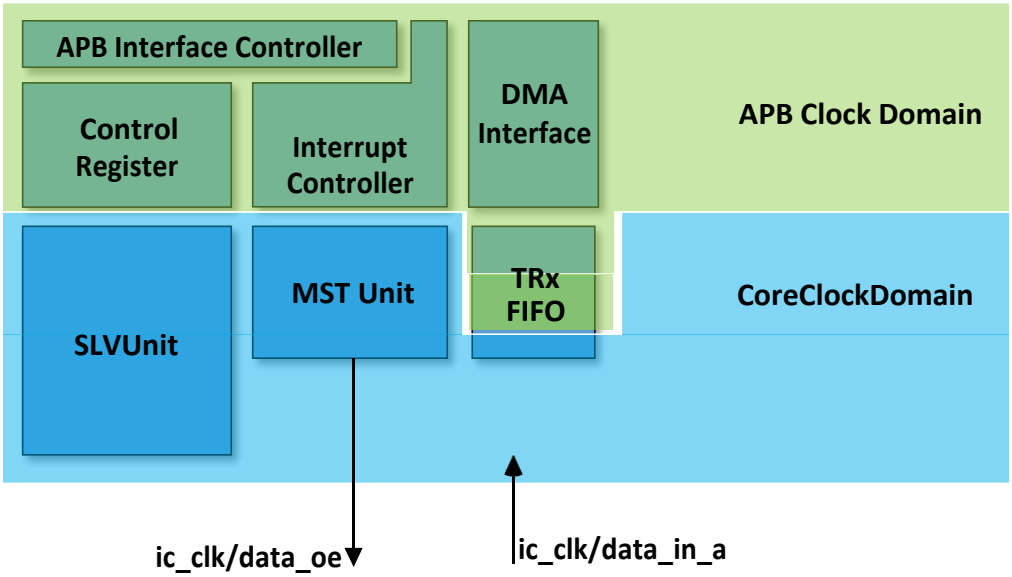


Figure 18. I2C Functional Diagram

7.8. PWM Interface

Pulse-Width Modulation (PWM) controllers generate pulse signals. The duty cycle, high time, and low time of pulse signals are programmable. In some particular applications, especially for LED and motor unit control, PWM is one of the most used interfaces. PWM interfaces can operate with GTimer, therefore PWM can work without involving the CPU.

PWM Features

- Supports maximum 8 PWM functions
- 0 ~100% duty can be configured
- Use selected HS GTimer interrupt as counter source
- Minimum resolution is 50ns
- The period could be configured up to 8 seconds

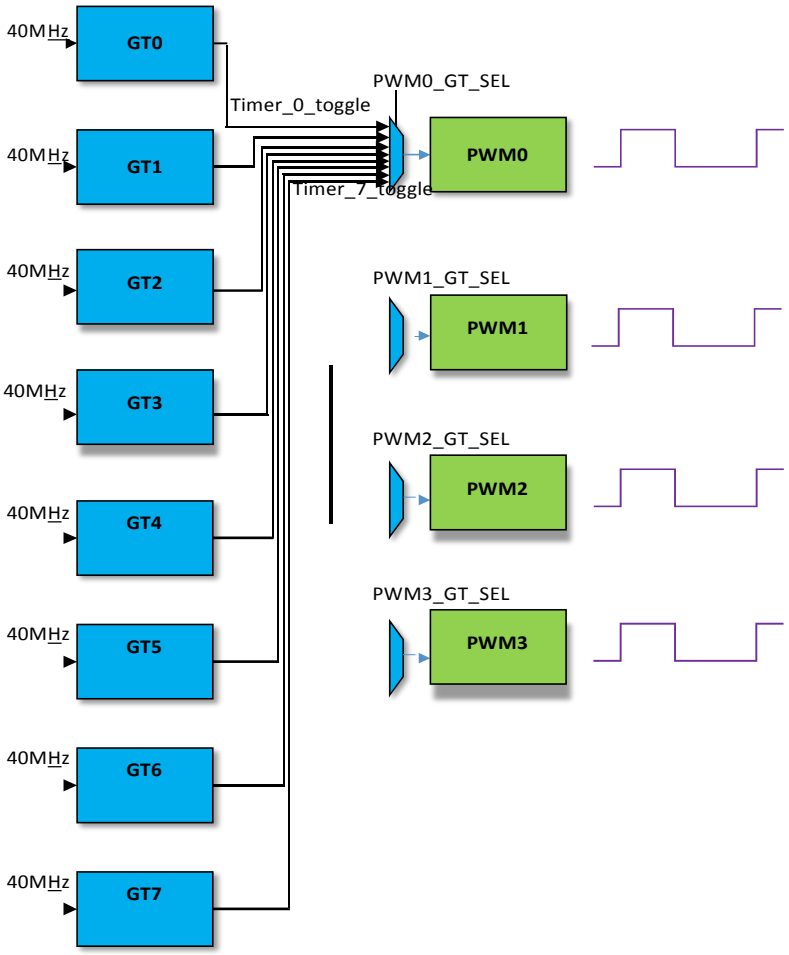


Figure 19. PWM Functional Diagram

7.9. Security Engine

In order to enhance security levels in embedded systems, the security engine offers various authentication and encryption/decryption functions to meet different states of security usage. A crypto engine provides low SW computing and high performance cryptographic operation (such as authentication, encryption, and decryption).

Security Engine Features

- Provides low SW computing and high performance encryption
- Supported authentication algorithms:
  - General cryptographic hash function
    - MD5
    - SAH1
    - SHA2-224
    - SHA2-256
    - Sequential hash
  - HMAC (Hash-based message authentication code)
    - HMAC_MD5
    - HMAC_SHA1
    - HMAC_SHA2-224
    - HMAC_SHA2-256
  - Cipher (Encryption/Decryption) algorithms
    - AES-128/192/256
      - ECB (Electronic Codebook) mode
      - CBC (Cipher Block Chaining) mode
      - CTR (Counter) mode
      - CFB (Cipher Feedback) mode
      - OFB (Output Feedback) mode
      - GCTR (Galois CTR) mode
      - GMAC (Galois MAC) mode
      - GHASH (Galois HASH) mode
      - GCM (Galois/Counter Mode) mode
  - CRC

8. RF Characteristics

Ameba ZII includes integrated WLAN RF transceiver architecture, and operates in 2.4 GHz WLAN and Bluetooth systems.

8.1. RF Block Diagram

This section describes the Ameba ZII RF block diagram. Ameba ZII includes a Wi-Fi/BT subsystem that integrates a Wi-Fi/BT modem sharing a front-end RF (ADC, TRSW, LPF, PA, LNA, etc.), and this chip is compatible with IEEE 802.11b/g/n protocol.

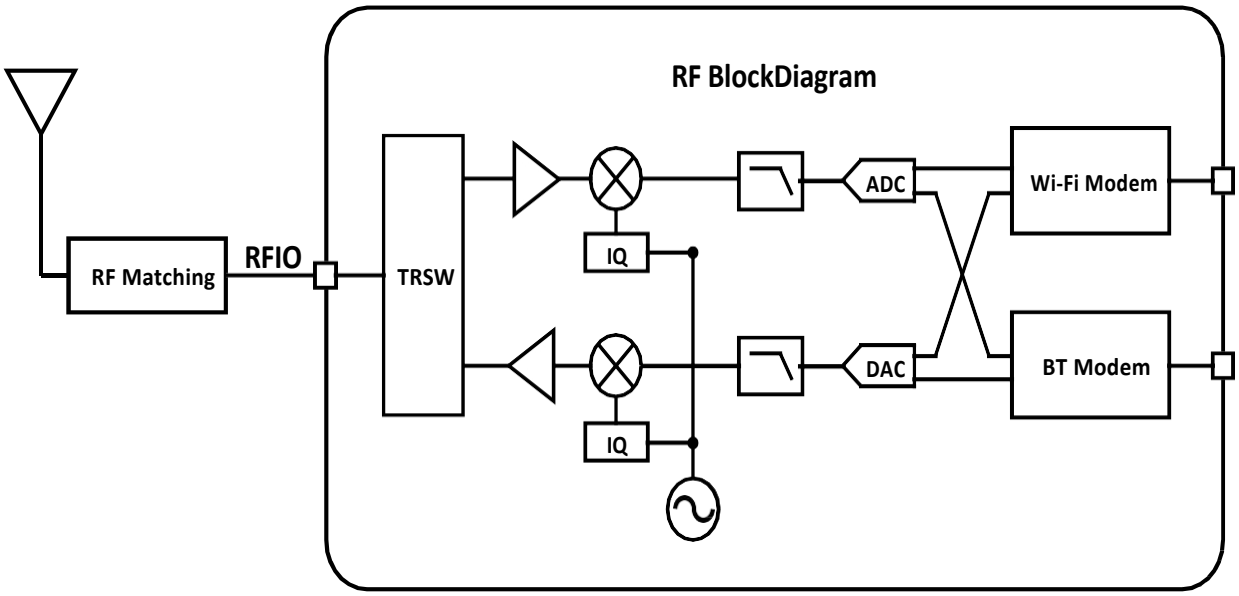


Figure 20. RF Block Diagram

8.2. Wi-Fi Radio Characteristics

Values in Table 16 are typical values, and the reference point is the antenna port including front-end loss. These values may change slightly depending on different RF front-end designs or PCB designs.

8.2.1. Wi-Fi 2.4GHz Band RF Receiver Specifications

Table 16. Wi-Fi 2.4GHz Band RF Receiver Specifications

Note: The above Rx performance values are based on 25 degree, 3.3V, 50ohm @LAB environment & Realtek EVB.

Parameter	Description	Min	Typ.	Max	Units
Frequency Range	-	2400	-	2500	MHz
802.11b RX Sensitivity (8% PER)	1 Mbps DSSS	-	-99.0	-	dBm
	2 Mbps DSSS	-	-95.5	-	dBm
	5.5 Mbps DSSS	-	-93.5	-	dBm
	11 Mbps DSSS	-	-90.0	-	dBm
802.11g RX Sensitivity (10% PER)	6 Mbps OFDM	-	-94.0	-	dBm
	9 Mbps OFDM	-	-93.0	-	dBm
	12 Mbps OFDM	-	-91.5	-	dBm
	18 Mbps OFDM	-	-89.0	-	dBm
	24 Mbps OFDM	-	-86.0	-	dBm
	36 Mbps OFDM	-	-82.5	-	dBm
	48 Mbps OFDM	-	-78.0	-	dBm
	54 Mbps OFDM	-	-76.5	-	dBm
802.11n RX Sensitivity (10% PER)	HT20 MCS0	-	-93.5	-	dBm
	HT20 MCS1	-	-91.0	-	dBm
	HT20 MCS2	-	-88.5	-	dBm
	HT20 MCS3	-	-85.5	-	dBm
	HT20 MCS4	-	-82.5	-	dBm
	HT20 MCS5	-	-77.0	-	dBm
	HT20 MCS6	-	-75.5	-	dBm
	HT20 MCS7	-	-74.0	-	dBm
Maximum Receive Level	1 Mbps DSSS	-	-	0	dBm
	6M bps OFDM	-	-	0	dBm

8.2.2. Wi-Fi 2.4GHz Band RF Transmitter Specifications

Table 17. Wi-Fi 2.4GHz Band RF Transmitter Specifications

Parameter	Description	Min	Typ.	Max	Units
Frequency Range	-	2400	-	2500	MHz
TX power	1 Mbps DSSS	-	21	-	dBm
	11 Mbps DSSS	-	21	-	dBm
	6 Mbps OFDM	-	19	-	dBm
	54 Mbps OFDM	-	17	-	dBm
	HT20 MCS0	-	19	-	dBm
	HT20 MCS7	-	16	-	dBm
TX EVM	1 Mbps DSSS	-	8	-	%
	11 Mbps DSSS	-	8	-	%
	6 Mbps OFDM	-	-5	-	dB
	54 Mbps OFDM	-	-25	-	dB
	HT20 MCS0	-	-5	-	dB
	HT20 MCS7	-	-28	-	dB
Carrier suppression	-	-	-	-30	dBc
Harmonic Output Power	2nd Harmonic	-	-	-45	dBm/MHz
	3rd Harmonic	-	-	-45	dBm/MHz

Note 1: The above Tx performance values are based on 25 degree, 3.3V, 50ohm @LAB environment & Realtek EVB.
Note 2: Target TX power is configurable based on different applications or certification requirements. Werecommend to back off 3dB for mass production pass rate, and include a corner case margin.

8.3. Bluetooth Radio Characteristic

Values in Table 18 and Table 19 are typical values, and the reference point is the antenna port including front-end loss. These values may change slightly depending on different RF front-end designs or PCB designs. Both the transmitter specifications and the receiver specifications follow Bluetooth SIG specifications.

8.3.1. BT RF Transmitter Specifications

Table 18. Bluetooth Transmitter Performance Table-BLE

Parameter	Description	Min	Typ.	Max	Units
Frequency Range	-	2402	-	2480	MHz
Tx Output Power	-	2.5	4.5	6.5	dBm
Adjacent channel transmit power	F = F0 ± 1 MHz	-	-15	-	dB
	F = F0 ± 2 MHz	-	-53	-	dB
	F = F0 ± 3 MHz	-	-56	-	dB
	F = F0 ± > 3 MHz	-	-57	-	dB
Δ f1avg	-	-	246	-	kHz
Δ f2max	-	-	220	-	kHz
Δ f2avg/Δ f1avg	-	-	0.92	-	-
ICFT	-	-	-15	-	KHz
Drift rate	-	-	2	-	kHz/50μs
Initial drift rate	-	-	-2	-	kHz

Note: The above Tx performance values are based on 25 degree, 3.3V, 50ohm @LAB environment & Realtek EVB.

8.3.2. BT RF Receiver Specifications

Table 19. Bluetooth Receiver Performance Table-BLE

Parameter	Description	Min	Typ.	Max	Units
Parameter	Description	Minimum	Typical	Maximum	Units
Frequency Range	-	2402	-	2480	MHz
Rx Sensitivity @30.8% PER	Without spur channel	-	-100	-	dBm
Maximum received signal @30.8% PER	-	0	-	-	dBm
Co-channel C/I Adjacent channel selectivity C/I	-	-	8	-	dB
	F = F0 + 1 MHz	-	-5	-	dB
	F = F0 - 1 MHz	-	-4	-	dB
	F = F0 + 2 MHz	-	-40	-	dB
	F = F0 - 2 MHz	-	-25	-	dB
	F = F0 + 3 MHz	-	-45	-	dB
	F = F0 - 3 MHz	-	-20	-	dB
Out-of-band blocking performance	30 MHz ~ 2000 MHz	-30	-	-	dBm
	2000 MHz ~ 2400 MHz	-35	-	-	dBm
	2500 MHz ~ 3000 MHz	-35	-	-	dBm
Intermodulation	3000 MHz ~ 12.5 GHz	-30	-	-	dBm

Note: The above Rx performance values are based on 25 degree, 3.3V, 50ohm @LAB environment & Realtek EVB.

9. Electrical Characteristics

9.1. Temperature Limit Ratings

Table 20. Temperature Limit Ratings

Parameter	Min	Max	Units
Storage Temperature	-55	+150	°C
Ambient Operating Temperature	-20	+85	°C
Ambient Operating Temperature (Wide)1	-40	+105	°C
Junction Temperature	0	+125	°C

Note 1: Only the RTL8720Cx-VT2-CG supports the wider temperature range.

9.2. Temperature Characteristics

Table 21. Thermal Properties

PCB (layer)	$T_{ambient}$(°C)	θ_{JA}(°C/W)	Ψ_{JT} (°C/W)	Ψ_{JB}(°C/W)
2	70	62.09	0.93	11.81

Note: The above values are based on the Realtek EVB.

9.3. Power Supply DC Characteristics

Table 22. Power Supply DC Characteristics

Parameter	Symbol	Min	Typ.	Max	Units
DC Supply Voltage for VDD_IN (3.3V)	VDD_IN	2.97	3.3	3.63	V
DC Supply Voltage for VDD_IN (5V)	VDD_IN	4.5	5	5.5	V
DC Supply Voltage for 3.3V Power Rail	VD33_SDIO VA33_XTAL VA33_SYN VA33_RF VA33_PA VA33_TR VD33_FLASH VD33_OUT	2.97	3.3	3.63	V
DC Supply Voltage for 1.1V Power Rail	VD11_CORE	1.09	1.146	1.20	V
DC Supply Voltage for GPIO/Embedded Flash	VD1833_LPC	2.97	3.3	3.63	V
DC Supply Voltage for Embedded PSRAM1	VD1833_LPC	1.7	1.8	1.95	V

Note: Only the RTL8720CM-VA2-CG/RTL8720CM-VT2-CG have an embedded PSRAM, VD1833_LPC needed to provide 1.8V for PSRAM power supply.

9.4. Digital IO Pin DC Characteristics

Table 23. Typical Digital IO DC Parameters

Symbol	Parameter	Conditions	Min	Typ.	Max	Units
V_{IH}	Input-High Voltage	LVTTL	2.0	-	-	V
V_{IL}	Input-Low Voltage	LVTTL	-	-	0.8	V
V_{OH}	Output-High Voltage	LVTTL	2.4	-	-	V
V_{OL}	Output-Low Voltage	LVTTL	-	-	0.4	V
V_{T+}	Schmitt-Trigger High Level	-	1.377	1.683	1.908	V
V_{T-}	Schmitt-Trigger Low Level	-	0.729	0.957	1.116	V
I_{IL}	Input-Leakage Current	VIN = 3.3V or 0	-10	±1	10	μA
-	Driving for Normal Pins	-	4	-	16	mA
I_{OH}	Driving for 5V UART Pins (GPIOA_13/GPIOA_14)	3.3V/5V	4/4	-	8/8	mA
I_{OL}	Driving for 5V UART Pins (GPIOA_13/GPIOA_14)	3.3V/5V	4/4	-	8/8	mA
-	Driving for SDIO Device Pins	-	4	-	16	mA
-	Loading for Normal Pins	-	-	15	-	pF
-	Loading for 5V UART Pins (GPIOA_13/GPIOA_14)		-	15	-	pF
-	Loading for SDIO Device Pins	-	-	15	-	pF
-	Pull Resistance for Normal Pins	3.3V	-	75	-	KΩ
-	Pull Resistance for 5V UART Pins (GPIOA_13/GPIOA_14)	3.3V/5V	-	80/120	-	KΩ
-	Pull Resistance for SDIO Device Pins	3.3V	-	50	-	KΩ

Note: The pull resistance values are typical values checked in the manufacturing process, and are not tested.

9.5. ESD Characteristics

Table 24. ESD Characteristics

Reliability Test	Standard	Test Condition	Result
Human Body Model (HBM)	JESD22-A114F-2008	±2000V	Pass
Machine Model (MM)	JESD22-A115C-2010	±100V	Pass
Charge Device Model (CDM)	JESD22-C101F-2013	±500V	Pass

9.6. Power State and Power Sequence

9.6.1. Power On or Resuming from Deep Sleep Sequence

The timing sequence of Power On or Resuming from Deep Sleep is given in Figure 21.

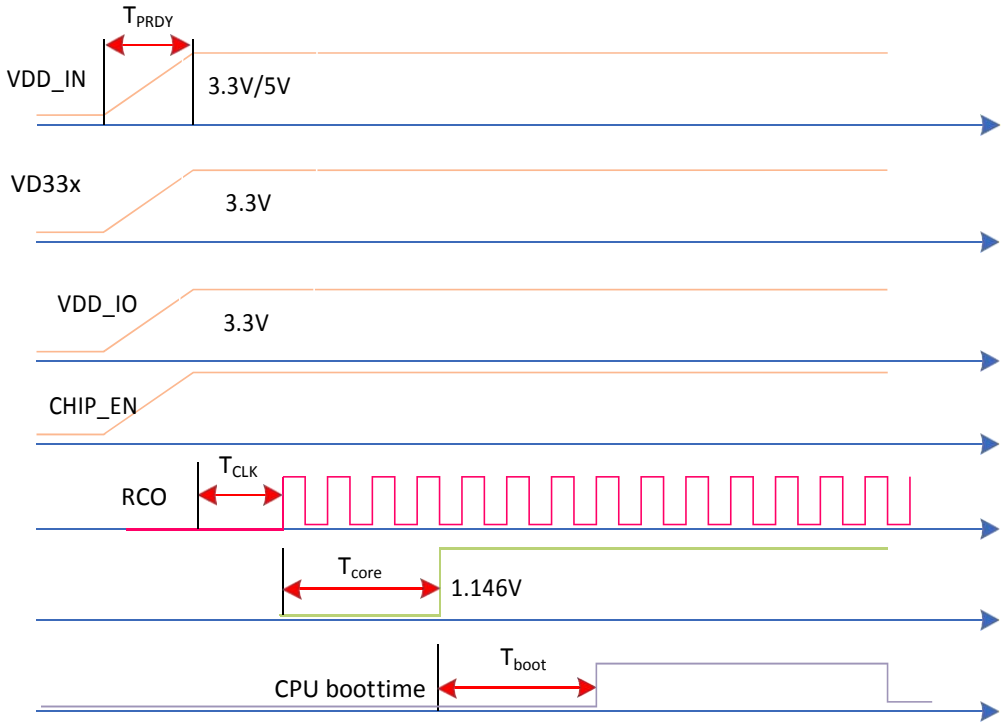


Figure 21. Power-On Sequence or Resume from Deep Sleep

Table 25. Timing Specification for Power on Sequence

Symbol	Parameter	Min	Typ.	Max	Units
T_{PRDY}	3.3V Ready Time	0.6	-	5	ms
T_{PRDY}	5V Ready Time	1	-	5	ms
T_{CLK}	Internal Ring Clock Stable Time after 3.3V Ready	1	-	-	ms
T_{core}	Core Power Ready Time	1.5	-	-	ms

9.6.2. Resume from Standby Mode Sequence

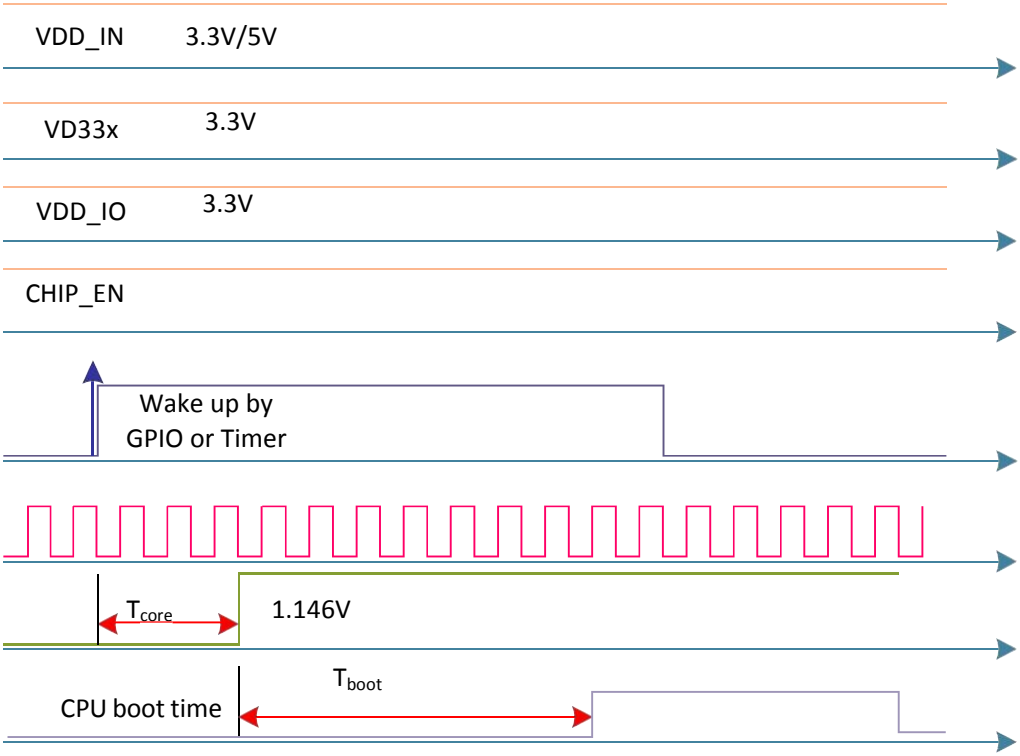


Figure 22. Timing Sequence Resume from Standby

Table 26. Timing Specification for Resume from Standby Mode Sequence

Symbol	Parameter	Min	Typ.	Max	Units
T_{core}	Core Power Ready Time	1.5	-	-	ms

9.6.3. Shutdown Sequence

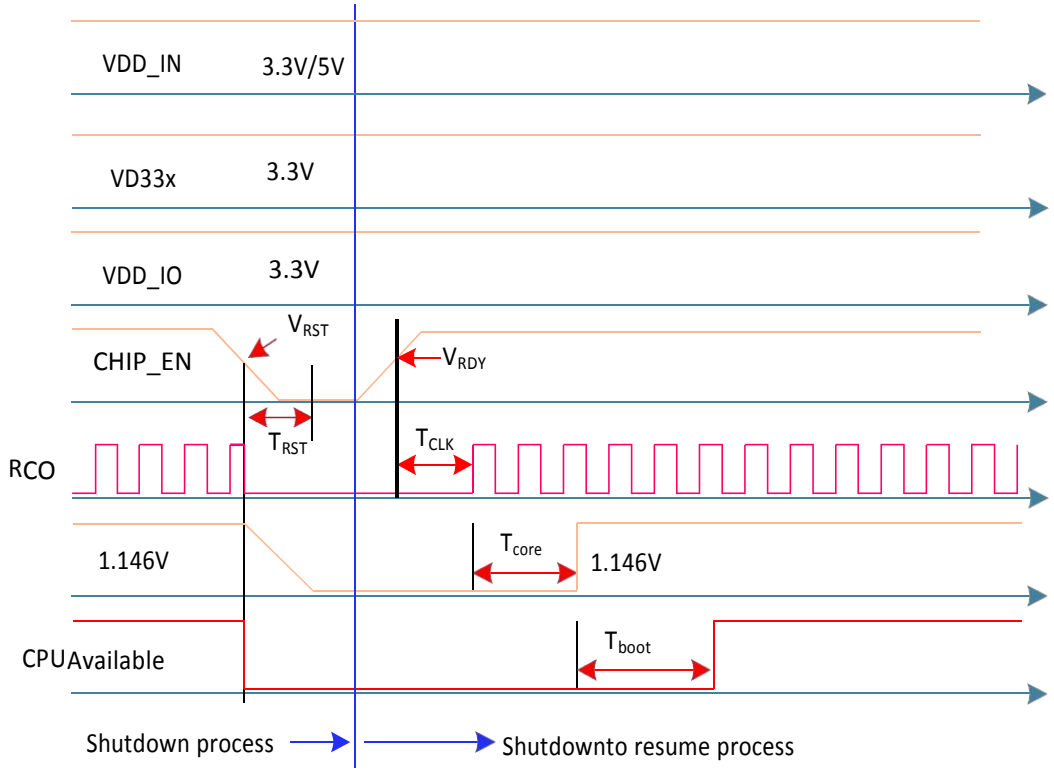


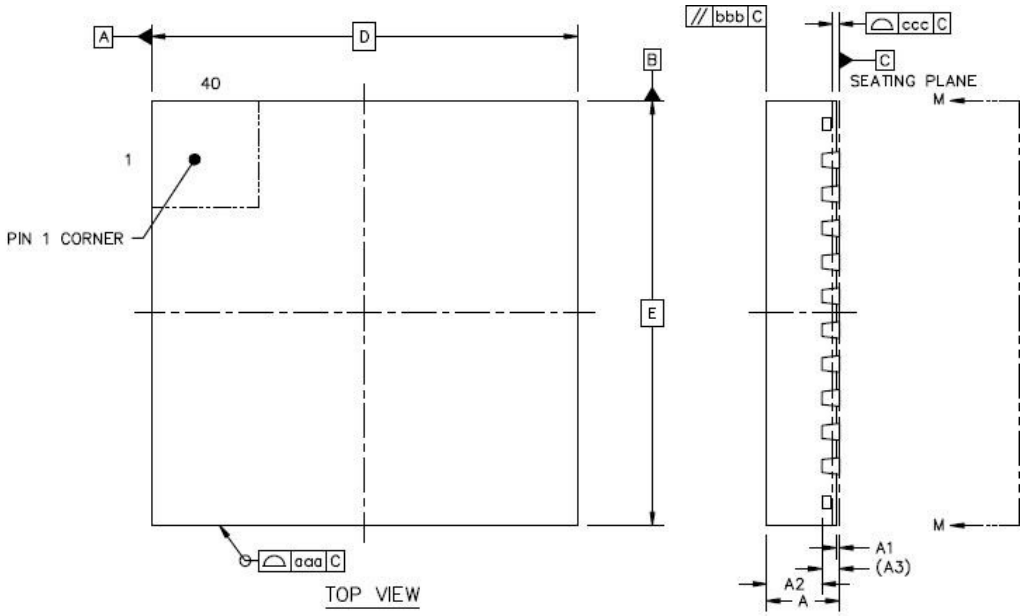
Figure 23. Timing Sequence of Shutdown

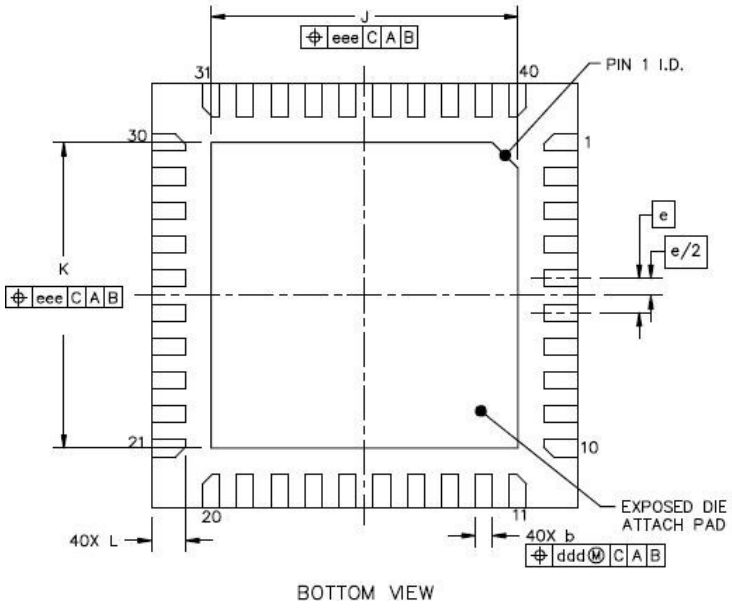
Table 27. Timing Specification for Shutdown Sequence

Symbol	Parameter	Min	Typ.	Max	Units
V_{RST}	Shutdown occurs after CHIP_EN is lower than this voltage	-	0.8	-	V
T_{RST}	The require time that CHIP_EN lower than V_{RST}	1	-	-	ms
V_{RDY}	Enable PMC after CHIP_EN higher than this voltage	2	-	-	V
T_{CLK}	Internal Ring Clock Stable Time after 3.3V ready	1	-	-	ms
T_{core}	Core Power Ready Time	1.5	-	-	ms

10. Mechanical Dimensions

10.1. Package Specification





10.2. Mechanical Dimensions Notes

Table 28. Mechanical Dimensions Notes

Symbol	Dimension in mm		
	Min	Nom.	Max
A	0.80	0.85	0.90
A_1	0.00	0.035	0.05
A_2	-	0.65	0.70
A_3	0.203 REF		
b	0.15	0.20	0.25
D/E	5.00 BSC		
e	0.40 BSC		
J	3.5	3.6	3.7
K	3.5	3.6	3.7
L	0.35	0.40	0.45

Note: CONTROLLING DIMENSION: MILLIMETER (mm). RFERENCE DOCUMENT: JEDEC MO-220.

11. Ordering Information

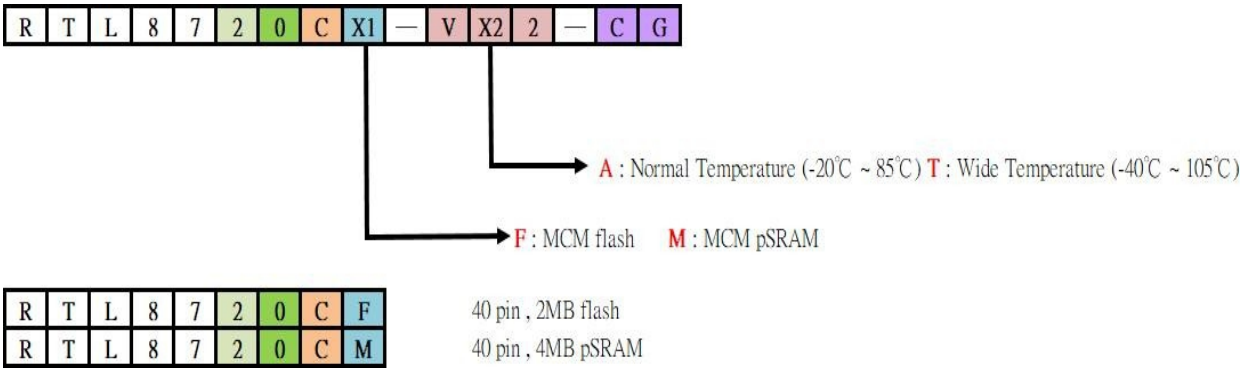


Table 29. Ordering Information

Part Number	Package
RTL8720CF-VA2-CG	QFN40, 'Green' Package. MCM 2MB Flash
RTL8720CM-VA2-CG	QFN40, 'Green' Package. MCM 4MB PSRAM
RTL8720CF-VT2-CG	QFN40, 'Green' Package. MCM 2MB Flash. Wide temp. range; see section 9.1, page 33
RTL8720CM-VT2-CG	QFN40, 'Green' Package. MCM 4MB PSRAM. Wide temp. range; see section 9.1, page 33

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